

8-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD78F9177 is μ PD789166 Subseries (small, general-purpose) in the 78K/0S Series.

The μ PD78F9177 replaces the internal ROM of the μ PD789166 with flash memory.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evolution stages of system development, small-scale production and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD789167, 789177, 789167Y, 789177Y Subseries User's Manual: U14186E

78K/0S Series User's Manual Instruction: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 24 Kbytes
- High-speed RAM: 512 bytes
- Minimum instruction execution time can be changed from high-speed (0.4 μ s: @5.0-MHz operation with main system clock) to ultra-low-speed (122 μ s: @ 32.768-kHz operation with subsystem clock)
- 10-bit resolution A/D converter: 6 channels
- I/O ports: 23
- Serial interface: 1 channel
 - 3-wire serial I/O mode / UART mode: 1 channel
- Timers: 6 channels
 - 16-bit timer: 1 channel
 - 8-bit timer/event counter: 2 channels
 - 8-bit timer: 1 channel
 - Watch timer: 1 channel
 - Watchdog timer: 1 channel
- On-chip 16-bit multiplier
- Power supply voltage: $V_{DD} = 4.5$ to 5.5 V

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

APPLICATIONS

Air-conditioner, White goods, etc

ORDERING INFORMATION

μPD78F9177CU

Part Number

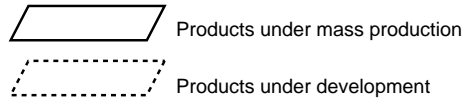
Package

μPD78F9177CU

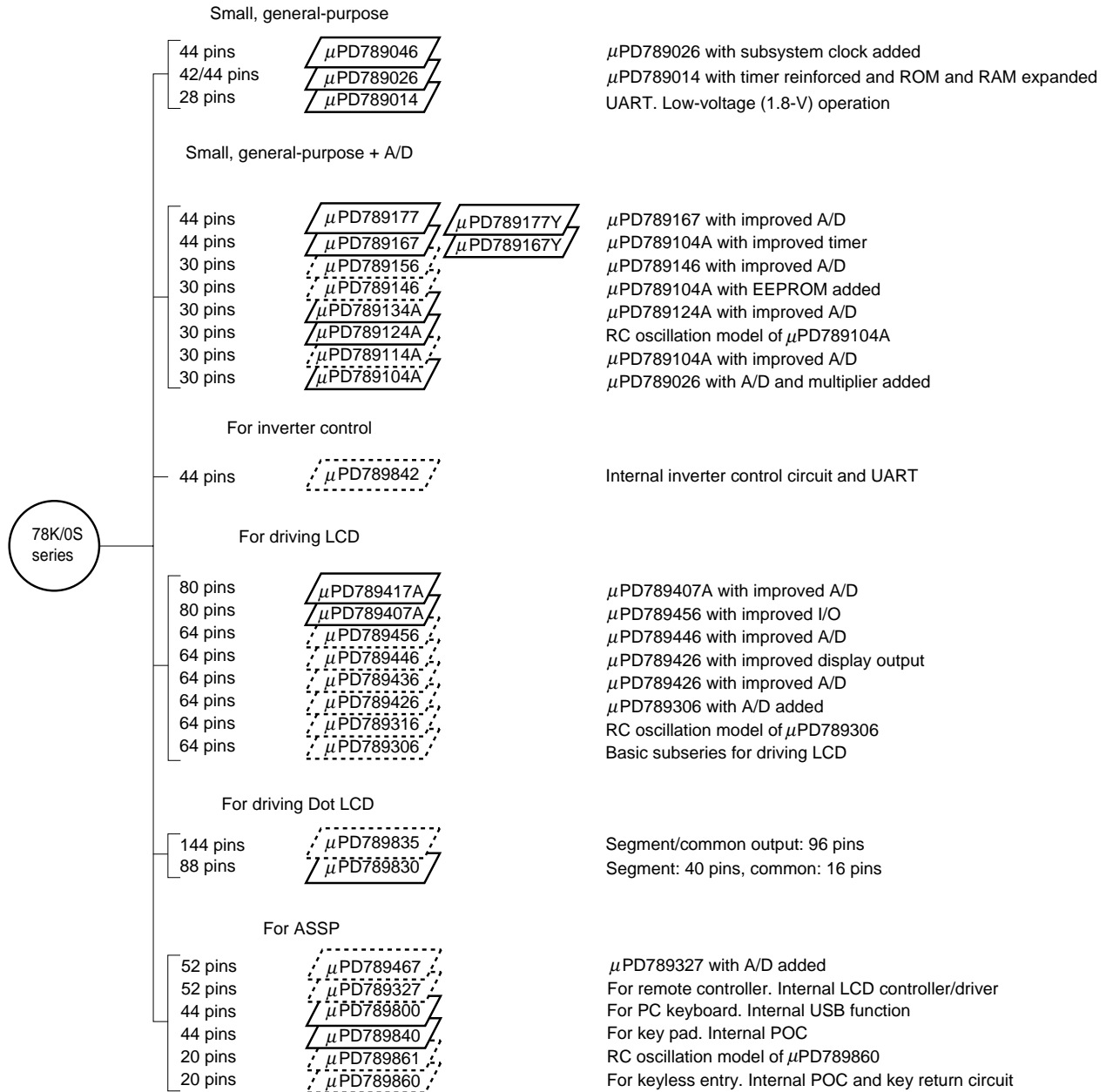
42-pin plastic SDIP(600 mil)

★ 78K/0S SERIES DEVELOPMENT

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Y subseries supports SMB.



The major differences between subseries are shown below.

Function Subseries Name		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	V _{DD} MIN Value	Remark	
			8-bit	16-bit	Watch	WDT							
Small, general- purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART:1 ch)	34 pins	1.8 V	–	
	μPD789026	4 K-16 K			–								
	μPD789014	2 K-4 K	2 ch	–						22 pins			
Small, general- purpose + A/D	μPD789177	16 K-24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31 pins	1.8 V	–	
	μPD789167						8 ch	–					
	μPD789156	8 K-16 K	1 ch	–	–	–	–	4 ch	20 pins			Internal EEPROM	
	μPD789146						4 ch	–					
	μPD789134A	2 K-8 K					–	4 ch					RC oscillation version
	μPD789124A						4 ch	–					
	μPD789114A						–	4 ch					
μPD789104A	4 ch						–						
For inverter control	μPD789842	8 K-16 K	3 ch	Note	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30 pins	4.0 V	–	
For LCD driving	μPD789417A	12 K-24 K	3 ch	1 ch	1 ch	1 ch	–	7 ch	1 ch (UART: 1 ch)	43 pins	1.8 V	–	
	μPD789407A						7 ch	–					
	μPD789456	12 K-16 K	2 ch				–	6 ch		30 pins			
	μPD789446						6 ch	–					
	μPD789436						–	6 ch					
	μPD789426	8 K to 16K					6 ch	–		40 pins			
	μPD789316						–	–					
μPD789306	–						–						
For Dot LCD driving	μPD789835	24 K-60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch	28 pins	1.8 V	–	
	μPD789830	24 K	1 ch	1 ch			–			30 pins	2.7 V		
ASSP	μPD789467	4 K-24 K	2 ch	–	1 ch	1 ch	1 ch	–	–	18 pins	1.8 V	Internal LCD	
	μPD789327						–		1 ch	21 pins			
	μPD789800	8 K	2 ch	1 ch	–	1 ch	–		2 ch (USB: 1 ch)	31 pins	4.0 V	–	
	μPD789840						4 ch		1 ch	29 pins	2.8 V		
	μPD789861	4 K		–			–		–	14 pins	1.8 V	RC oscillation version, Internal EEPROM	
μPD789860	–						–		Internal EEPROM				

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		μPD78F9177CU						
Internal memory	Flash memory	24 Kbytes						
	High-speed RAM	512 bytes						
Minimum instruction execution time		<ul style="list-style-type: none"> • 0.4/1.6 μs (@5.0-MHz operation with main system clock) • 122 μs (@ 32.768-kHz operation with subsystem clock) 						
General-purpose registers		8 bits × 8 registers						
Instruction set		<ul style="list-style-type: none"> • 16-bit operations • Bit manipulations (set, reset, test) 						
Multiplier		8 bits × 8 bits = 16 bits						
I/O ports		<table border="0"> <tr> <td>Total:</td> <td style="text-align: right;">23</td> </tr> <tr> <td>• CMOS I/O:</td> <td style="text-align: right;">17</td> </tr> <tr> <td>• N-ch open drain:</td> <td style="text-align: right;">6</td> </tr> </table>	Total:	23	• CMOS I/O:	17	• N-ch open drain:	6
Total:	23							
• CMOS I/O:	17							
• N-ch open drain:	6							
A/D converters		10-bit resolution × 8 channels						
Serial interfaces		3-wire serial I/O/UART : 1 channel						
Timers		<ul style="list-style-type: none"> • 16-bit timer:1 channel • 8-bit timer/event counter:2 channels • 8-bit timer:1 channel • Watch timer:1 channel • Watchdog timer:1 channel 						
Timer output		4 output						
Buzzer output		1						
Vectored interrupt sources	Maskable	Internal: 10, External: 4						
	Non-maskable	Internal: 1						
Power supply voltage		V _{DD} = 4.5 to 5.5 V						
Operating ambient temperature		T _A = -40°C to +85°C						
Package		42-pin plastic SDIP (600 mil)						

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1. PIN CONFIGURATION (TOP VIEW)

- 42-pin plastic shrink DIP (600mil)
μPD78F9177CU

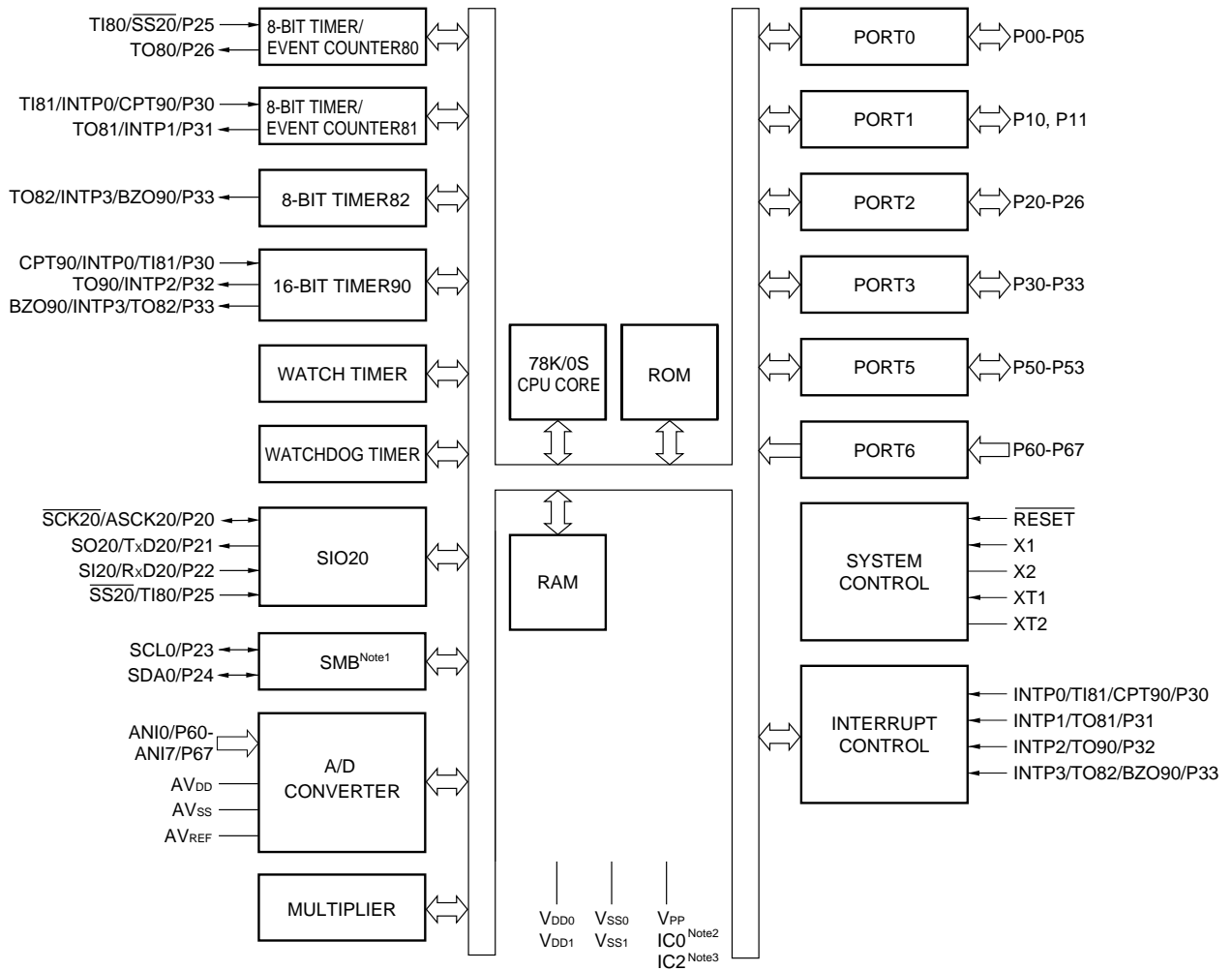
Vss0	1	42	X1
Vdd0	2	41	X2
TI80/SS20/P25	3	40	RESET
TO80/P26	4	39	XT1
P00	5	38	XT2
P01	6	37	Vpp
P02	7	36	P24
P03	8	35	P23
P04	9	34	P22/SI20/RxD20
Vss1	10	33	P21/SO20/TxD20
P05	11	32	Vdd1
P50	12	31	P20/SCK20/ASCK20
P51	13	30	P33/TO82/INTP3/BZO90
P52	14	29	P32
P53	15	28	P31/INTP1/TO81
Avvd	16	27	P30/CPT90/INTP0/TI81
Avref	17	26	P11
ANI0	18	25	P10
ANI1	19	24	Avss
ANI2	20	23	ANI5
ANI3	21	22	ANI4

Note

- Cautions**
1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1}.
 2. Connect the AV_{DD} pin to V_{DD0}.
 3. Connect the AV_{SS} pin to V_{SS0}.

ANI0 to ANI5:	Analog Input	$\overline{\text{RESET}}$:	Reset
ASCK20:	Asynchronous Serial Input	RxD20:	Receive Data
AV _{DD} :	Analog Power Supply	$\overline{\text{SCK20}}$:	Serial Clock (for SIO20)
AV _{REF} :	Analog Reference Voltage		Serial Clock
AV _{SS} :	Analog Ground		Serial Data
BZO90:	Buzzer Output	SI20:	Serial Input
CPT90:	Capture Trigger Input	SO20:	Serial Output
INTP0 to INTP3:	Interrupt from Peripherals	SS20:	Chip Select Input
P00 to P05:	Port 0	TI80, TI81:	Timer Input
P10, P11:	Port 1	TO80 to TO82, TO90:	Timer Output
P20 to P26:	Port 2	TxD20:	Transmit Data
P30 to P33:	Port 3	V _{DD0} , V _{DD1} :	Power Supply
P50 to P53:	Port 5	V _{PP} :	Programming Power Supply
		V _{SS0} , V _{SS1} :	Ground
		X1, X2:	Crystal (Main System Clock)
		XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



NOTES: Port 6, IC0, IC2, ANI7 and ANI6 are not available.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P10, P11	I/O	Port 1 2-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P20	I/O	Port 2 7-bit input/output port Input/output mode can be specified in 1-bit units For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by software. Only P23 and P24 can be used as N-ch open-drain input/output port pins.	Input	SCK20/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				
P24				
P25				TI80/SS20
P26				TO80
P30	I/O	Port 3 4-bit input/output port Input/output mode can be specified in 1-bit units On-chip pull-up resistor can be specified by software.	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain input/output port Input/output mode can be specified in 1-bit units	Input	–

Note

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
SCK20	I/O	Serial clock input/output for serial interface	Input	P20/ASCK20
SS20	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/SCK20
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer/event counter (TM80)	Input	P25/SS20
TI81	Input	External count clock input to 8-bit timer/event counter (TM81)	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer/event counter (TM80) output	Input	P26
TO81	Output	8-bit timer/event counter (TM81) output	Input	P31/INTP1
TO82	Output	8-bit timer (TM82) output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer (TM90) output	Input	P32/INTP2
BZO90	Output	16-bit timer (TM90) Buzzer output	Input	P33/INTP3/TO82
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
ANI0 to ANI5	Input	A/D converter analog input	Input	P60 to P67
AVREF	–	A/D converter reference voltage	–	–
AVSS	–	A/D converter ground potential	–	–
AVDD	–	A/D converter analog power supply	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
VDD0	–	Positive power supply	–	–
VDD1	–	Positive power supply (other than ports)	–	–
VSS0	–	Ground potential	–	–
VSS1	–	Ground potential (other than ports)	–	–
RESET	Input	System reset input	Input	–
VPP	–	Sets flash memory programming mode. Applies high voltage when a program is written or verified. Connect directly to VSS0 or VSS1 in normal operation mode.	–	–

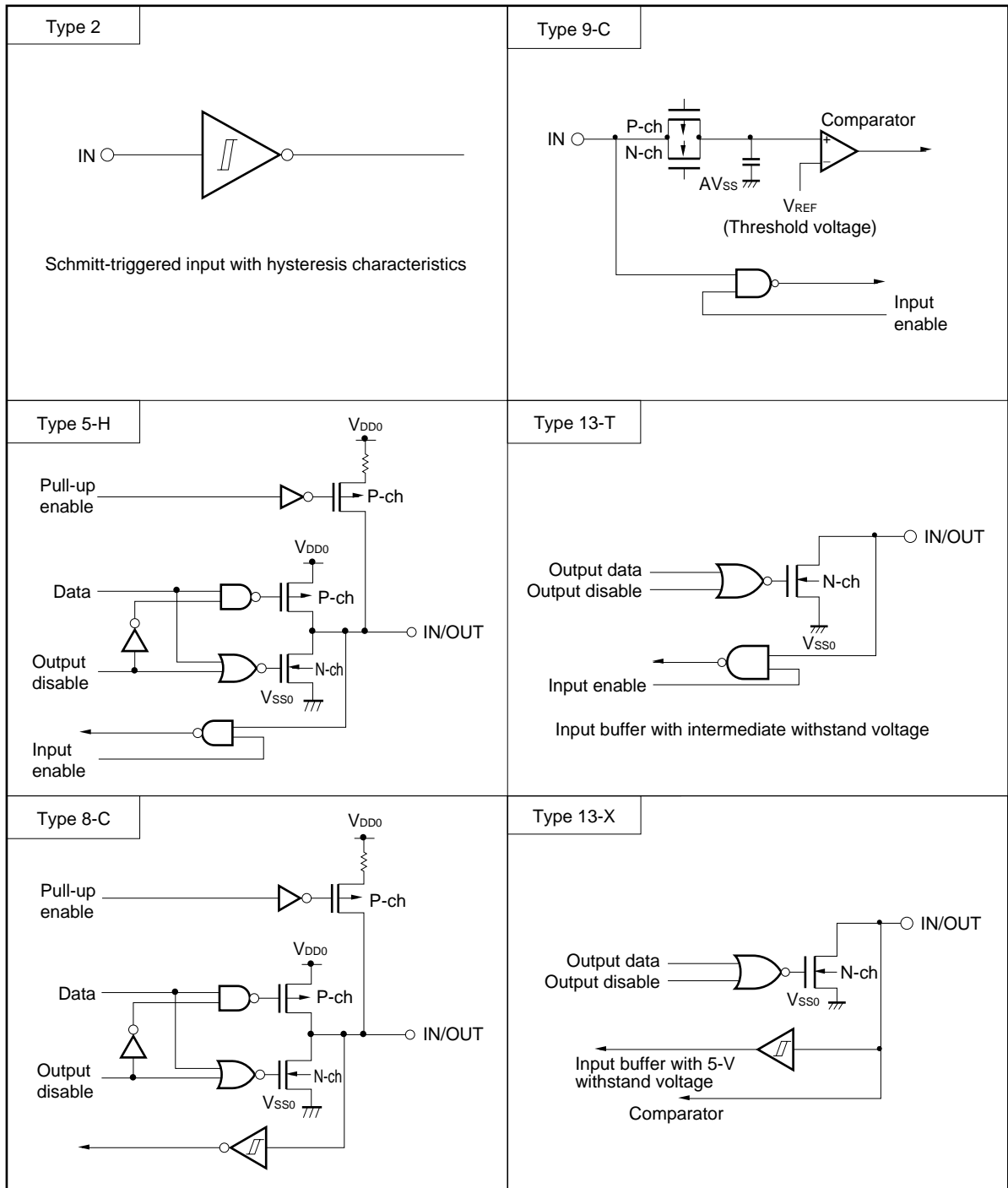
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins is shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Type of I/O Circuit for Each Pin and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins			
P00 to P05	5-H	I/O	Input: Independently connects to V_{DD0} , V_{DD1} or V_{SS0} , V_{SS1} via a resistor. Output: Leave open.			
P10, P11						
P20/SCK20/ASCK20	8-C		Input: Independently connects to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.			
P21/SO20/TxD20						
P22/SI20/RxD20						
P23	13-X			Input: Independently connects to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.		
P24						
P25/TI80/SS20	8-C				Input: Independently connects to V_{DD0} , V_{DD1} or V_{SS0} , V_{SS1} via a resistor. Output: Leave open.	
P26/TO80						
P30/INTP0/TI81/CPT90						
P31/INTP1/TO81						
P32/INTP2/TO90						
P33/INTP3/TO82/BZO90						
P50 to P53	13-T	Input: Independently connects to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.				
P60/ANI0 to P65/ANI5	9-C		Input			Connect directly to V_{DD0} , V_{DD1} or V_{SS0} , V_{SS1} .
XT1	-		Input			Connect to V_{SS0} or V_{SS1} .
XT2			-			Leave open.
RESET	2		Input	-		
V_{PP}	-		-	Connect directly to V_{SS0} or V_{SS1} .		

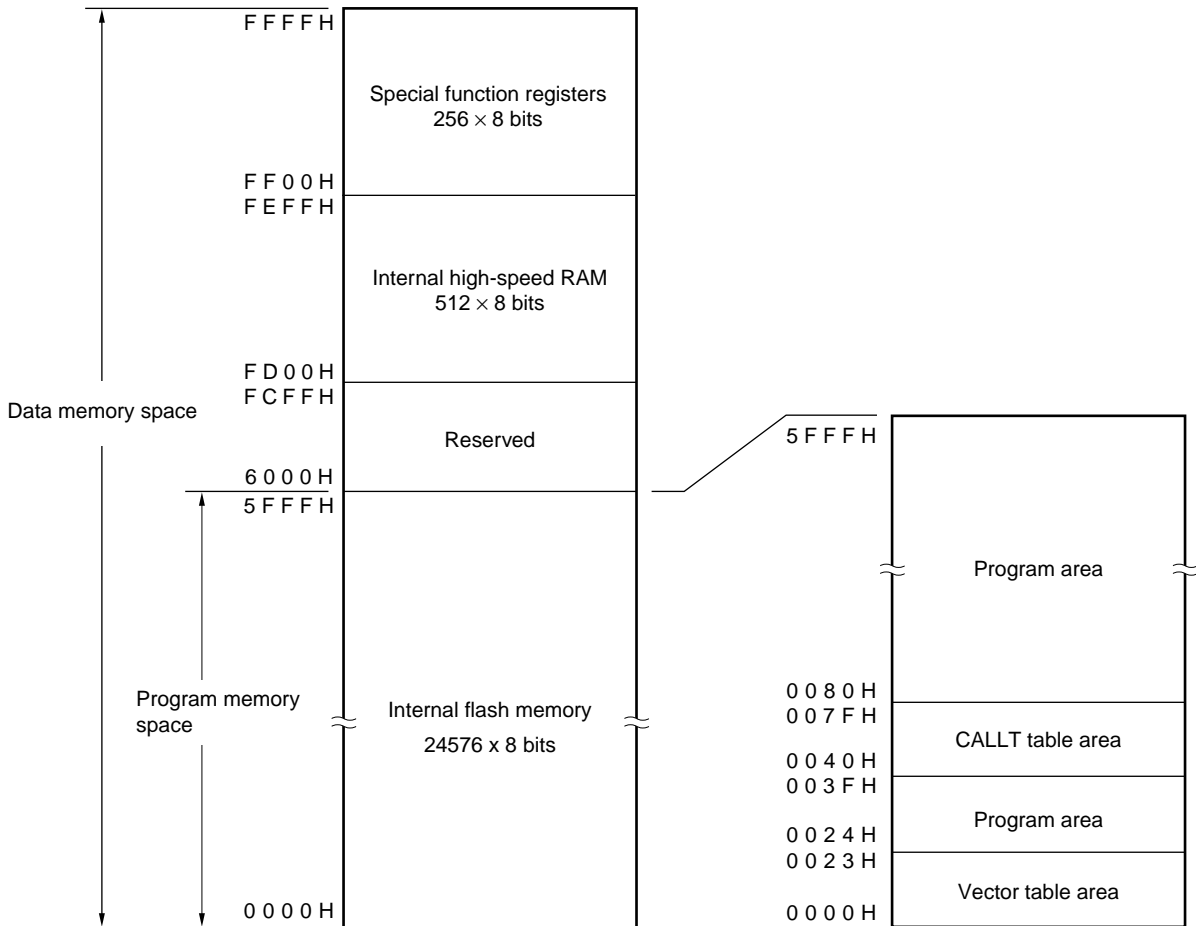
Figure 3-1. Pin Input/Output Circuits



4. CPU ARCHITECTURE

Products in the μPD78F9177 and μPD78F9177Y can access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. FLASH MEMORY PROGRAMMING

The on-chip program memory in the μPD78F9177 is flash memory.

The flash memory can be written with the μPD78F9177 mounted on the target system (on-board). Connect the dedicated flash programmer (Flashpro III (part number: FL-PR3, PG-FP3)) to the host machine and target system to write the flash memory.

Remark FL-PR3 is made by Naito Densai Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

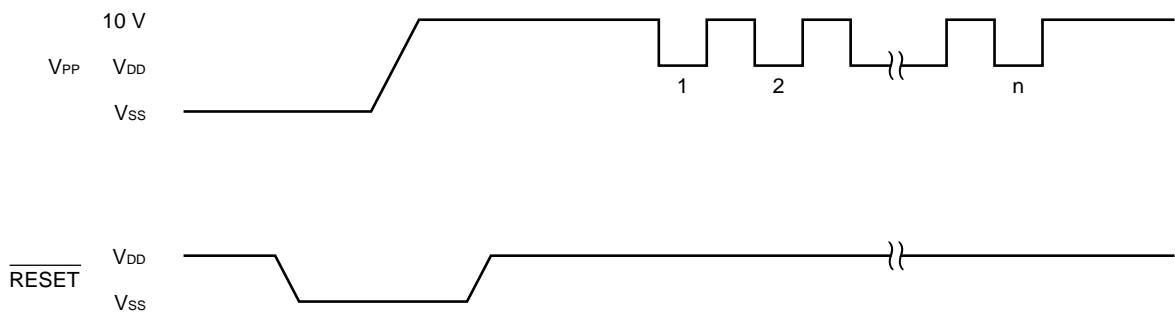
The flash memory is written by using Flashpro III and by means of serial communication. Select a communication mode from those listed in Table 5-1. To select a communication mode, the format shown in Figure 5-1 is used. Each communication mode is selected by the number of V_{PP} pulses shown in Table 5-1.

Table 5-1. Communication Mode

Communication	Pins Used	Number of Vpp Pulses
3-wire serial I/O	SCK20/ASCK20/P20 SO20/TxD20/P21 SI20/RxD20/P22	0
UART	TxD20/SO20/P21 RxD20/SI20/P22	8
Pseudo 3-wire mode Note1	P00(Serial clock input) P01(Serial data output) P02(Serial data input)	12

Note 1.Serial transfer is performed by controlling a port by software.

Figure 5-1. Communication Mode Selection Format



5.2 Function of Flash Memory Programming

By transmitting/receiving commands and data in the selected communication mode, operations such as writing to the flash memory are performed. Table 5-2 shows the major functions of flash memory programming.

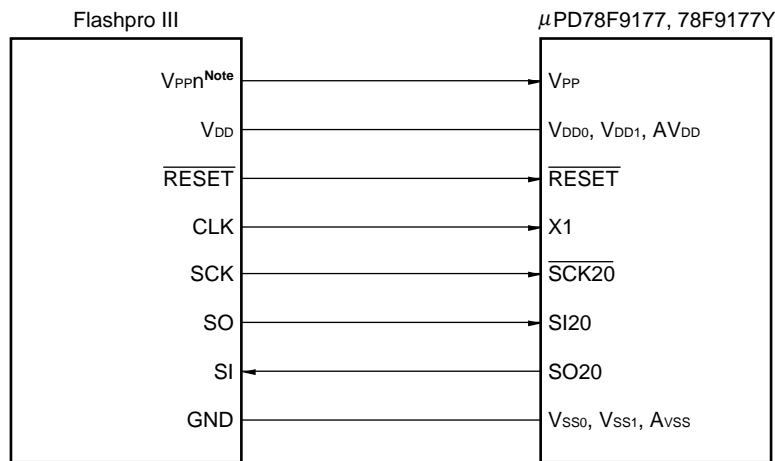
Table 5-2. Functions of Flash Memory Programming

Function	Description
Batch erase	Erases all contents of memory
Batch blank check	Checks erased state of entire memory
Data write	Write to flash memory based on write start address and number of data written (number of bytes)
Batch verify	Compares all contents of memory with input data

5.3 Flashpro III Connection Example

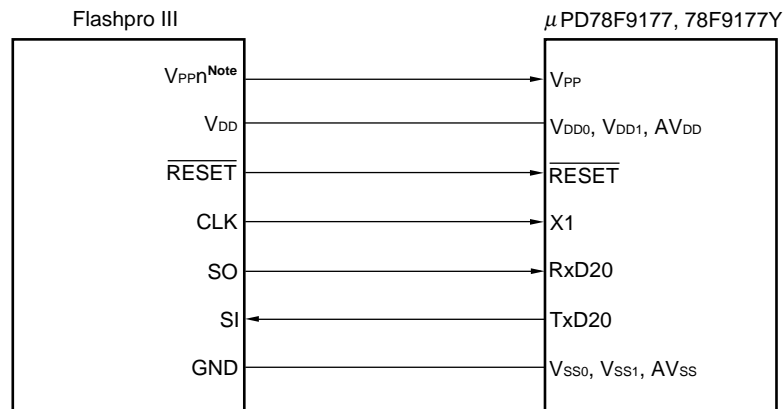
How the Flashpro III is connected to the μPD78F9177 differs depending on the communication mode (3-wired serial I/O, UART, or pseudo 3-wire mode). Figures 5-2 to 5-5 show the connection in the respective mode.

Figure 5-2. Flashpro III Connection in 3-wired Serial I/O Mode



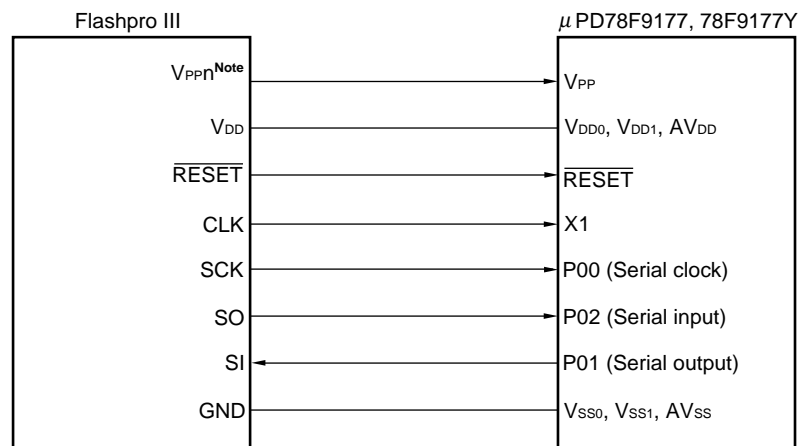
Note n = 1, 2

Figure 5-4. Flashpro III Connection in UART Mode



Note n = 1, 2

Figure 5-5. Flashpro III Connection in Pseudo Serial I/O Mode (When Port 0 is Used)



Note n = 1, 2

5.4 Example of Settings for Flashpro III (PG-FP3)

Set as follows when writing to flash memory using the Flashpro III (PG-FP3).

<1> Download the parameter file.

<2> Select the serial mode and the serial clock using the type command.

<3> the following is a setting example using the PG-FP3.

Table 5-3. Example Using PG-FP3

Communication mode	Setting example using PG-FP3		Number of Vpp pulses Note1
3-wired serial I/O mode	COMM PORT	SIO ch-0	0
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943MHz	
	SIO CLK	1.0MHz	
	In Flashpro	4.0MHz	
SIO CLK		1.0MHz	
UART	COMM PORT	UART-ch0	8
	CPU CLK	On target board	
		On target board	
	UART BPS	9600/19200/76800 bps	
Pseudo 3-wire mode	COMM PORT	Port A	12
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943MHz	
	SIO CLK	1.0MHz	
	In Flashpro	4.0MHz	
SIO CLK		1.0MHz	

Notes 1. The number of V_{PP} pulses supplied from the Flashpro III during serial communication initialization. The pins to be used in communication are determined by this number of pulses.

Remark COMM PORT: Selection of serial port
 SIO CLK : Selection of serial clock frequency
 CPU CLK : Selection of CPU clock source to be input

6. INSTRUCTION SET OVERVIEW

This section lists the μPD78F9177 instruction set.

6.1 Conventions

6.1.1 Operand identifiers and description methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, \$, and [], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- \$: Relative address specification
- !: Absolute address specification
- []: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, \$, or [] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 6-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7), AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH immediate data or label FE20H to FF1FH immediate data or label (even address only)
addr16 addr5	0000H to FFFFH immediate data or label (Only even addresses for 16-bit data transfer instructions) 0040H to 007FH immediate data or label (even address only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

6.1.2 Descriptions of the operation field

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC registers pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Non-maskable interrupt servicing flag
():	Memory contents indicated by address or register contents in parentheses
X _H , X _L :	Higher 8 bits and lower 8 bits of 16-bit register
^:	Logical product (AND)
∨:	Logical sum (OR)
⊕:	Exclusive OR
⌘:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

6.1.3 Description of the flag operation field

(Blank):	Not affected
0:	Cleared to 0
1:	Set to 1
×	Set/cleared according to the result
R:	Previously saved value is restored

6.2 Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
MOV	r, #byte	3	6	$r \leftarrow \text{byte}$			
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow \text{byte}$			
	sfr, #byte	3	6	$\text{sfr} \leftarrow \text{byte}$			
	A, r ^{Note 1}	2	4	$A \leftarrow r$			
	r, A ^{Note 1}	2	4	$r \leftarrow A$			
	A, saddr	2	4	$A \leftarrow (\text{saddr})$			
	saddr, A	2	4	$(\text{saddr}) \leftarrow A$			
	A, sfr	2	4	$A \leftarrow \text{sfr}$			
	sfr, A	2	4	$\text{sfr} \leftarrow A$			
	A, laddr16	3	8	$A \leftarrow (\text{addr16})$			
	laddr16, A	3	8	$(\text{addr16}) \leftarrow A$			
	PSW, #byte	3	6	$\text{PSW} \leftarrow \text{byte}$	x	x	x
	A, PSW	2	4	$A \leftarrow \text{PSW}$			
	PSW, A	2	4	$\text{PSW} \leftarrow A$	x	x	x
	A, [DE]	1	6	$A \leftarrow (\text{DE})$			
	[DE], A	1	6	$(\text{DE}) \leftarrow A$			
	A, [HL]	1	6	$A \leftarrow (\text{HL})$			
	[HL], A	1	6	$(\text{HL}) \leftarrow A$			
	A, [HL + byte]	2	6	$A \leftarrow (\text{HL} + \text{byte})$			
[HL + byte], A	2	6	$(\text{HL} + \text{byte}) \leftarrow A$				
XCH	A, X	1	4	$A \leftrightarrow X$			
	A, r ^{Note 2}	2	6	$A \leftrightarrow r$			
	A, saddr	2	6	$A \leftrightarrow (\text{saddr})$			
	A, sfr	2	6	$A \leftrightarrow (\text{sfr})$			
	A, [DE]	1	8	$A \leftrightarrow (\text{DE})$			
	A, [HL]	1	8	$A \leftrightarrow (\text{HL})$			
	A, [HL + byte]	2	8	$A \leftrightarrow (\text{HL} + \text{byte})$			
MOVW	rp, #word	3	6	$\text{rp} \leftarrow \text{word}$			
	AX, saddrp	2	6	$\text{AX} \leftarrow (\text{saddrp})$			
	saddrp, AX	2	8	$(\text{saddrp}) \leftarrow \text{AX}$			
	AX, rp ^{Note 3}	1	4	$\text{AX} \leftarrow \text{rp}$			
	rp, AX ^{Note 3}	1	4	$\text{rp} \leftarrow \text{AX}$			

- Notes**
1. Except r = A
 2. Except r = A, X
 3. Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp ^{Note}	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, laddr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, laddr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A - byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) - byte	×	×	×
	A, r	2	4	A, CY ← A - r	×	×	×
	A, saddr	2	4	A, CY ← A - (saddr)	×	×	×
	A, laddr16	3	8	A, CY ← A - (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A - (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A - (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A - byte - CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) - byte - CY	×	×	×
	A, r	2	4	A, CY ← A - r - CY	×	×	×
	A, saddr	2	4	A, CY ← A - (saddr) - CY	×	×	×
	A, laddr16	3	8	A, CY ← A - (addr16) - CY	×	×	×
	A, [HL]	1	6	A, CY ← A - (HL) - CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A - (HL + byte) - CY	×	×	×

Note Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{cpu}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	$A \leftarrow A \wedge \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \wedge \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \wedge r$	×		
	A, saddr	2	4	$A \leftarrow A \wedge (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \wedge (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \wedge (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \wedge (\text{HL} + \text{byte})$	×		
OR	A, #byte	2	4	$A \leftarrow A \vee \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \vee (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \vee (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee (\text{HL} + \text{byte})$	×		
XOR	A, #byte	2	4	$A \leftarrow A \oplus \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \oplus \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \oplus r$	×		
	A, saddr	2	4	$A \leftarrow A \oplus (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \oplus (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \oplus (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \oplus (\text{HL} + \text{byte})$	×		
CMP	A, #byte	2	4	$A - \text{byte}$	×	×	×
	saddr, #byte	3	6	$(\text{saddr}) - \text{byte}$	×	×	×
	A, r	2	4	$A - r$	×	×	×
	A, saddr	2	4	$A - (\text{saddr})$	×	×	×
	A, !addr16	3	8	$A - (\text{addr16})$	×	×	×
	A, [HL]	1	6	$A - (\text{HL})$	×	×	×
	A, [HL + byte]	2	6	$A - (\text{HL} + \text{byte})$	×	×	×
ADDW	AX, #word	3	6	$AX, CY \leftarrow AX + \text{word}$	×	×	×
SUBW	AX, #word	3	6	$AX, CY \leftarrow AX - \text{word}$	×	×	×
CMPW	AX, #word	3	6	$AX - \text{word}$	×	×	×
INC	r	2	4	$r \leftarrow r + 1$	×	×	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) + 1$	×	×	
DEC	r	2	4	$r \leftarrow r - 1$	×	×	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) - 1$	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
INCW	rp	1	4	$rp \leftarrow rp + 1$			
DECW	rp	1	4	$rp \leftarrow rp - 1$			
ROR	A, 1	1	2	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
ROL	A, 1	1	2	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
RORC	A, 1	1	2	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
ROLC	A, 1	1	2	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×
SET1	saddr.bit	3	6	$(saddr.bit) \leftarrow 1$			
	sfr.bit	3	6	$sfr.bit \leftarrow 1$			
	A.bit	2	4	$A.bit \leftarrow 1$			
	PSW.bit	3	6	$PSW.bit \leftarrow 1$	×	×	×
	[HL].bit	2	10	$(HL).bit \leftarrow 1$			
CLR1	saddr.bit	3	6	$(saddr.bit) \leftarrow 0$			
	sfr.bit	3	6	$sfr.bit \leftarrow 0$			
	A.bit	2	4	$A.bit \leftarrow 0$			
	PSW.bit	3	6	$PSW.bit \leftarrow 0$	×	×	×
	[HL].bit	2	10	$(HL).bit \leftarrow 0$			
SET1	CY	1	2	$CY \leftarrow 1$			1
CLR1	CY	1	2	$CY \leftarrow 0$			0
NOT1	CY	1	2	$CY \leftarrow \overline{CY}$			×
CALL	!addr16	3	6	$(SP - 1) \leftarrow (PC + 3)_H, (SP - 2) \leftarrow (PC + 3)_L,$ $PC \leftarrow addr16, SP \leftarrow SP - 2$			
CALLT	[addr5]	1	8	$(SP - 1) \leftarrow (PC + 1)_H, (SP - 2) \leftarrow (PC + 1)_L,$ $PC_H \leftarrow (00000000, addr5 + 1)$ $PC_L \leftarrow (00000000, addr5)$ $SP \leftarrow SP - 2$			
RET		1	6	$PC_H \leftarrow (SP + 1), PC_L \leftarrow (SP),$ $SP \leftarrow SP + 2$			
RETI		1	8	$PC_H \leftarrow (SP + 1), PC_L \leftarrow (SP),$ $PSW \leftarrow (SP + 2), SP \leftarrow SP + 3,$ $NMIS \leftarrow 0$	R	R	R
PUSH	PSW	1	2	$(SP - 1) \leftarrow PSW, SP \leftarrow SP - 1$			
	rp	1	4	$(SP - 1) \leftarrow rp_H, (SP - 2) \leftarrow rp_L,$ $SP \leftarrow SP - 2$			
POP	PSW	1	4	$PSW \leftarrow (SP), SP \leftarrow SP + 1$	R	R	R
	rp	1	6	$rp_H \leftarrow (SP + 1), rp_L \leftarrow (SP),$ $SP \leftarrow SP + 2$			
MOVW	SP, AX	2	8	$SP \leftarrow AX$			
	AX, SP	2	6	$AX \leftarrow SP$			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
BR	laddr16	3	6	$PC \leftarrow \text{addr16}$			
	\$addr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$			
	AX	1	6	$PC_H \leftarrow A, PC_L \leftarrow X$			
BC	\$addr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if CY = 1			
BNC	\$addr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if CY = 0			
BZ	\$addr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if Z = 1			
BNZ	\$addr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if Z = 0			
BT	saddr.bit, \$saddr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if (saddr. bit) = 1			
	sfr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if sfr. bit = 1			
	A.bit, \$saddr16	3	8	$PC \leftarrow PC + 3 + \text{jdisp8}$ if A. bit = 1			
	PSW.bit \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if PSW. bit = 1			
BF	saddr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if (saddr. bit) = 0			
	sfr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if sfr. bit = 0			
	A.bit, \$saddr16	3	8	$PC \leftarrow PC + 3 + \text{jdisp8}$ if A. bit = 0			
	PSW.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if PSW. bit = 0			
DBNZ	B, \$addr16	2	6	B ← B - 1, then $PC \leftarrow PC + 2 + \text{jdisp8}$ if B ≠ 0			
	C, \$addr16	2	6	C ← C - 1, then $PC \leftarrow PC + 2 + \text{jdisp8}$ if C ≠ 0			
	saddr, \$addr16	3	8	(saddr) ← (saddr) - 1, then $PC \leftarrow PC + 3 + \text{jdisp8}$ if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set Stop Mode			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

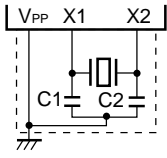
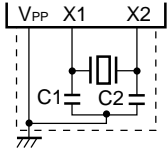
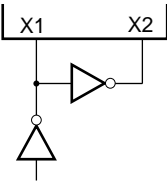
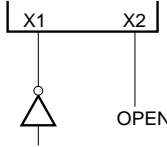
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}	$AV_{DD} - 0.3\text{ V} \leq V_{DD} \leq AV_{DD} + 0.3\text{ V}$	-0.3 to +6.5	V
	AV _{DD}	$AV_{REF} \leq AV_{DD} + 0.3\text{ V}$		V
	AV _{REF}	$AV_{REF} \leq V_{DD} + 0.3\text{ V}$		V
	V _{PP}		-0.3 to +10.5	V
Input voltage	V _{I1}	Pins other than P50 to P53, P23, P24	-0.3 to V _{DD} + 0.3	V
	V _{I2}	P23, P24	-0.3 to +5.5	V
	V _{I3}	P50 to P53	-0.3 to +13	V
Output voltage	V _O		-0.3 to V _{DD} + 0.3	V
Output current, high	I _{OH}	Per pin	-10	mA
		Total for all pins	-30	mA
Output current, low	I _{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T _A	In normal operation mode	-40 to +85	°C
		During flash memory programming	+10 to +40	°C
Storage temperature	T _{stg}		-40 to +125	°C

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Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) Note 1	V _{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V _{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f _x) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2				10	ms
External clock		X1 input frequency (f _x) Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})		85		500	ns
		X1 input frequency (f _x) Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})		85		500	ns

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

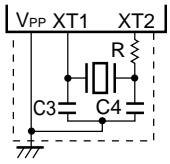
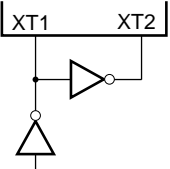
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f _{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2			1.2	2	S
External clock		XT1 input frequency (f _{XT}) Note 1		32		35	KHz
		XT1 input high-/low-level width (t _{XTH} , t _{XTL})		14.3		15.6	μs

- Notes**
1. Indicates only oscillator characteristics. Refer **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I _{OH}	Per pin				-1	mA
		Total for all pins				-15	mA
Output current, low	I _{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V _{IH1}	P00 to P05, P10, P11		0.7 V _{DD}		V _{DD}	V
	V _{IH2}	P50 to P53		0.7 V _{DD}		12	V
	V _{IH3}	RESET, P20 to P26, P30 to P33		0.8 V _{DD}		V _{DD}	V
	V _{IH4}	X1, X2, XT1, XT2		V _{DD} - 0.5		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P05, P10, P11		0		0.3 V _{DD}	V
	V _{IL2}	P50 to P53		0		0.3 V _{DD}	V
	V _{IL3}	RESET, P20 to P26, P30 to P33		0		0.2 V _{DD}	V
	V _{IL4}	X1, X2, XT1, XT2		0		0.4	V
Output voltage, high	V _{OH}	Pins other than P23, P24, P50 to P53	I _{OH} = -1 mA	V _{DD} - 1.0			V
			I _{OH} = -100 μA	V _{DD} - 0.5			V
Output voltage, low	V _{OL1}	Pins other than P50 to P53	I _{OL} = 10 mA			1.0	V
			I _{OL} = 400 μA			0.5	V
	V _{OL2}	P50 to P53	I _{OL} = 10 mA			1.0	V
			I _{OL} = 1.6 mA			0.4	V
Input leakage current, high	I _{LIH1}	V _I = V _{DD}	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			3	μA
	X1, X2, XT1, XT2				20	μA	
	I _{LIH3}	V _I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I _{LIL1}	V _I = 0 V	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			-3	μA
	I _{LIL2}		X1, X2, XT1, XT2			-20	μA
	I _{LIL3}		P50 to P53 (N-ch open drain)			-3 Note	μA
Output leakage current, high	I _{LOH}	V _O = V _{DD}				3	μA
Output leakage current, low	I _{LOL}	V _O = 0 V				-3	μA
Software pull-up resistor	R ₁	V _I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ

Note A low-level input leakage current of -60 μA(MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 and P50 to P53 are set to input mode. At times other than this, -3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply current	I _{DD1} Note 1	5.0-MHz crystal oscillation operating mode (C1 = C2 = 22pF)	V _{DD} = 5.0 V ± 10% Note 4	5.0	15.0	mA
	I _{DD2} Note 1	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22pF)	V _{DD} = 5.0 V ± 10% Note 4	2.0	6.0	mA
	I _{DD3} Note 1	32.768-kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22pF, R = 220kΩ)	V _{DD} = 5.0 V ± 10%	250	750	μA
	I _{DD4} Note 1	32.768-kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22pF, R = 220kΩ)	V _{DD} = 5.0 V ± 10%	50	150	μA
	I _{DD5} Note 1	32.768-kHz crystal stop STOP mode	V _{DD} = 5.0 V ± 10%	0.1	30	μA
	I _{DD6} Note 2	5.0-MHz crystal oscillation A/D operating mode (C1 = C2 = 22pF)	V _{DD} = 5.0 V ± 10% Note 4	6.0	17.0	mA

- Notes**
1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and the port current (including the current flowing through the internal pull-up resistors) are not included.
 2. The AV_{REF}On (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) are not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.
 3. When the main system clock is stopped.
 4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)
 5. During low-speed mode operation (when PCC is set to 02H)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T _{CY}	Operation based on the main system clock	0.4		8	μs
		Operation based on the subsystem clock	114	122	125	μs
TI80 and TI81 input frequency	f _{TI}		0		4	MHz
TI80 and TI81 input high-/low-level width	t _{TIH} , t _{TIL}		0.1			μs
Interrupt input high- /low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP3	10			μs
RESET input low- level width	t _{RSL}		10			μs
CPT90 input high- /low-level width	t _{CPH} ,		10			μs
	t _{CPL}					

(2) Serial interface (T_A = -40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

(a) 3-wire serial I/O mode (SCK20...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK20 cycle time	t _{KCY1}		800			ns
SCK20 high-/low-level width	t _{KH1} , t _{KL1}		t _{KCY1} /2-50			ns
SI20 setup time (to SCK20 ↑)	t _{SIK1}		150			ns
SI20 hold time (from SCK20 ↑)	t _{KSH1}		400			ns
SO20 output delay time from SCK20 ↓	t _{KSO1}	R = 1 kΩ, C = 100 pF Note	0		250	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode (SCK20...External clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK20 cycle time	t _{KCY2}		900			ns
SCK20 high-/low-level width	t _{KH2} , t _{KL2}		400			ns
SI20 setup time (to SCK20 ↑)	t _{SIK2}		100			ns
SI20 hold time (from SCK20 ↑)	t _{KSI2}		400			ns
SO20 output delay time from SCK20 ↓	t _{KSO2}	R = 1 kΩ, C = 100 pF Note	0		300	ns
SO20 setup time (when using SS20, to SS20 ↓)	t _{KAS2}				120	ns
SO20 disable time (when using SS20, from SS20 ↑)	t _{KDS2}				240	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

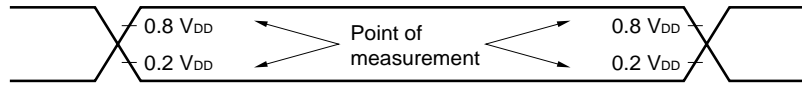
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

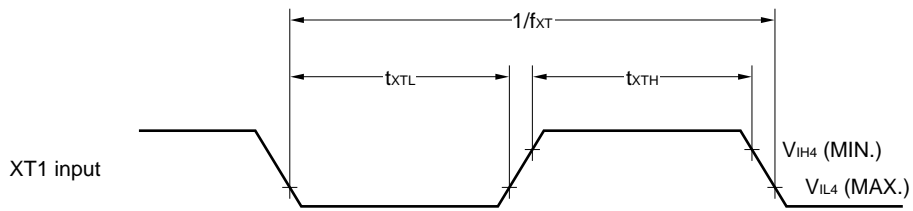
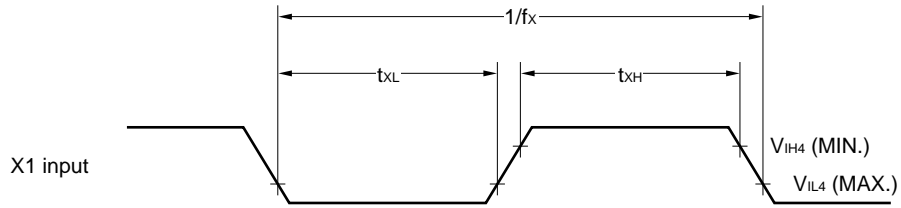
(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{CY3}		900			Ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			Ns
Transfer rate					39063	Bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

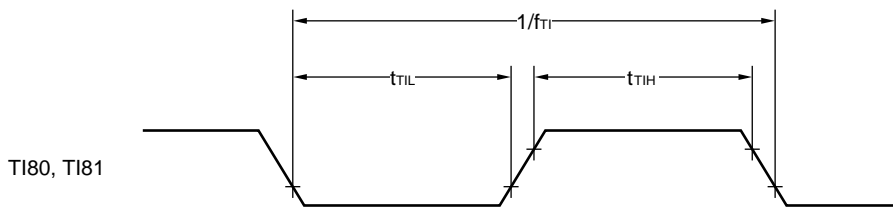
AC Timing Measurement Points (excluding the X1 and XT1 inputs)



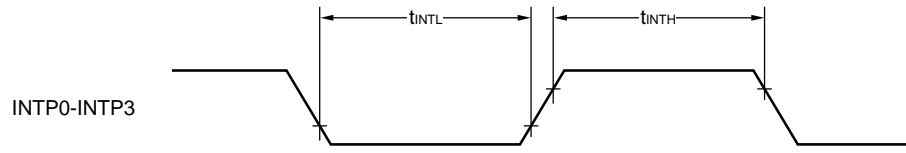
Clock Timing



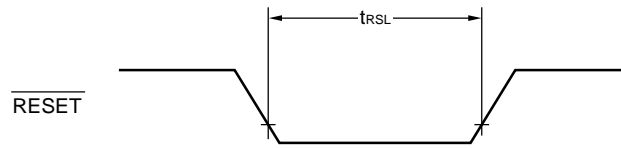
TI Timing



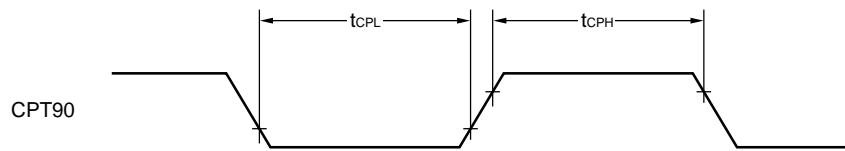
Interrupt Input Timing



RESET Input Timing

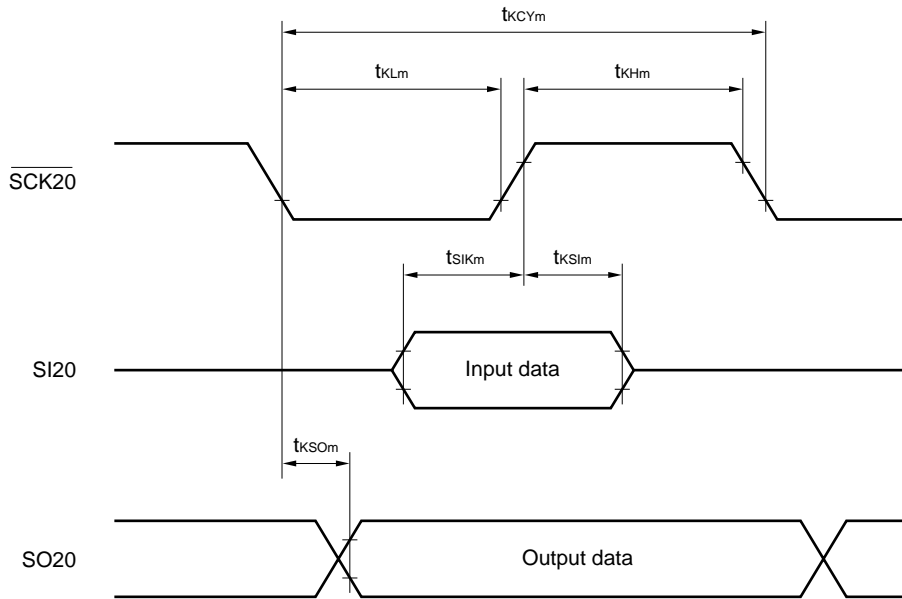


CPT90 Input Timing



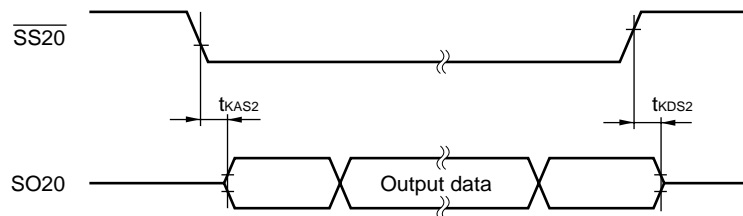
Serial Transfer Timing

3-wire serial I/O mode:

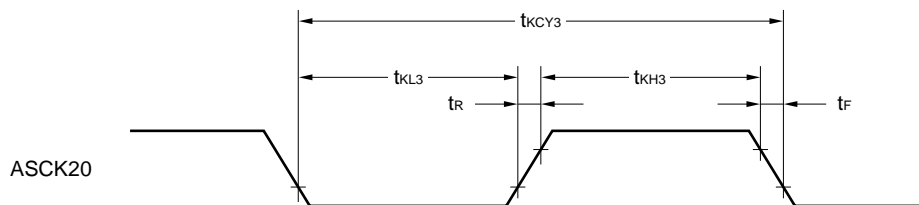


Remark $m = 1, 2$

3-wire serial I/O mode (when using $\overline{\text{SS20}}$):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = -40 to +85 °C, 4.5 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error Note		4.5 V ≤ AV _{REF} ≤ AV _{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
Conversion time	t _{CONV}	4.5 V ≤ AV _{REF} ≤ AV _{DD} ≤ 5.5 V	14		100	μs
Zero-scale error Note		4.5 V ≤ AV _{REF} ≤ AV _{DD} ≤ 5.5 V			±0.4	%FSR
Full-scale error Note		4.5 V ≤ AV _{REF} ≤ AV _{DD} ≤ 5.5 V			±0.4	%FSR
Integral linearity error Note	INL	4.5 V ≤ AV _{REF} ≤ AV _{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error Note	DNL	4.5 V ≤ AV _{REF} ≤ AV _{DD} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V _{IAN}		0		AV _{REF}	V
Reference voltage	AV _{REF}		4.5		AV _{DD}	V
Resistance between AV _{REF} and AV _{SS}	RA _{IREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

FLASH MEMORY WRITE/DELETE CHARACTERISTICS (T_A = 10 to 40 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V _{DD} pin) Note	I _{DDW}	When V _{PP} supply voltage = V _{PP1} (5.0-MHz crystal oscillation operation mode)			18	mA
Write current (V _{PP} pin) Note	I _{PPW}	When V _{PP} supply voltage = V _{PP1}			7.5	mA
Delete current (V _{DD} pin) Note	I _{DDE}	When V _{PP} supply voltage = V _{PP1} (5.0-MHz crystal oscillation operation mode)			18	mA
Delete current (V _{PP} pin) Note	I _{PPE}	When V _{PP} supply voltage = V _{PP1}			100	mA
Unit delete time	t _{er}		0.5	1	1	s
Total delete time	t _{era}				20	s
Write count		Delete/write are regarded as 1 cycle			20	Times
V _{PP} supply voltage	V _{PP0}	In normal operation	0		0.2V _{DD}	V
	V _{PP1}	During flash memory programming	9.7	10.0	10.3	V

Note The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and AV_{DD} current are not included.

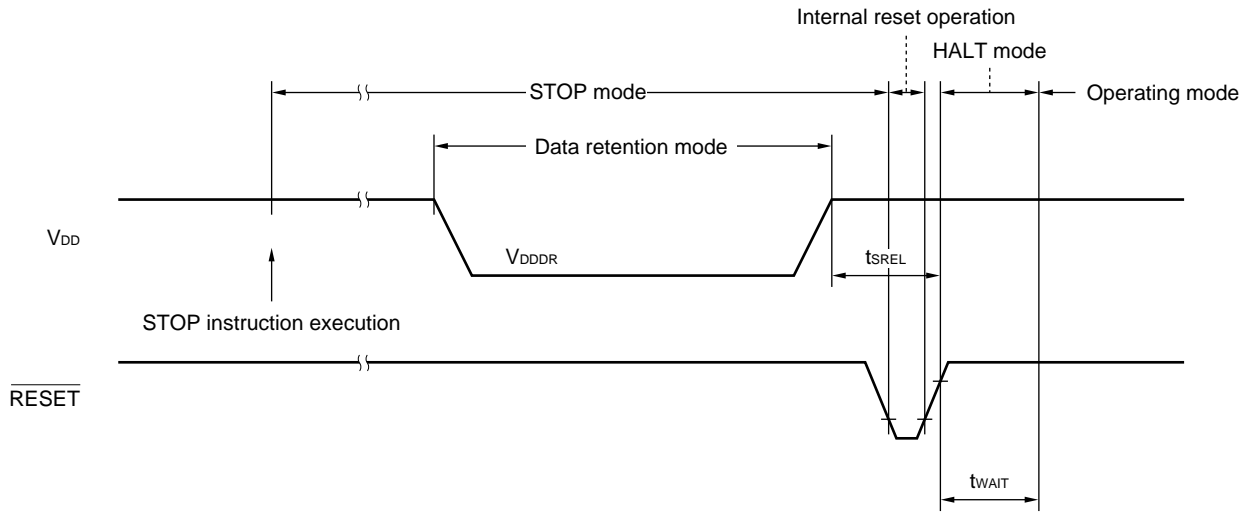
Data Memory Stop Mode Low Power Supply Voltage Data Retention Characteristics (T_A = -40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V _{DDDR}		4.5		5.5	V
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time Note 1	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁵ /f _x		s
		Release by interrupt request		Note 2		s

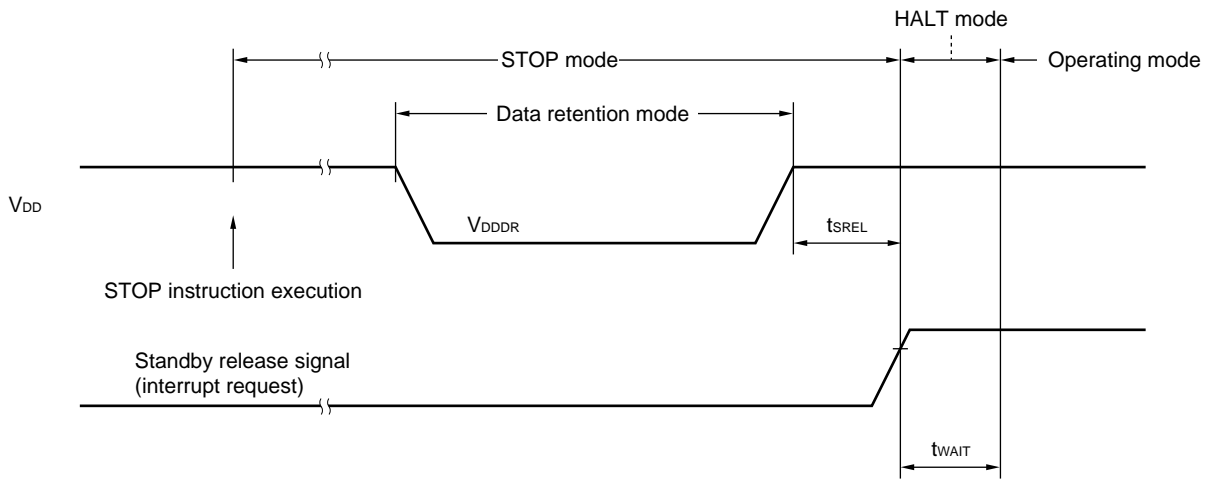
- Notes**
1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.
 2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), 2¹²/f_x, 2¹⁵/f_x, or 2¹⁷/f_x can be selected.

Remark f_x: Main system clock oscillation frequency

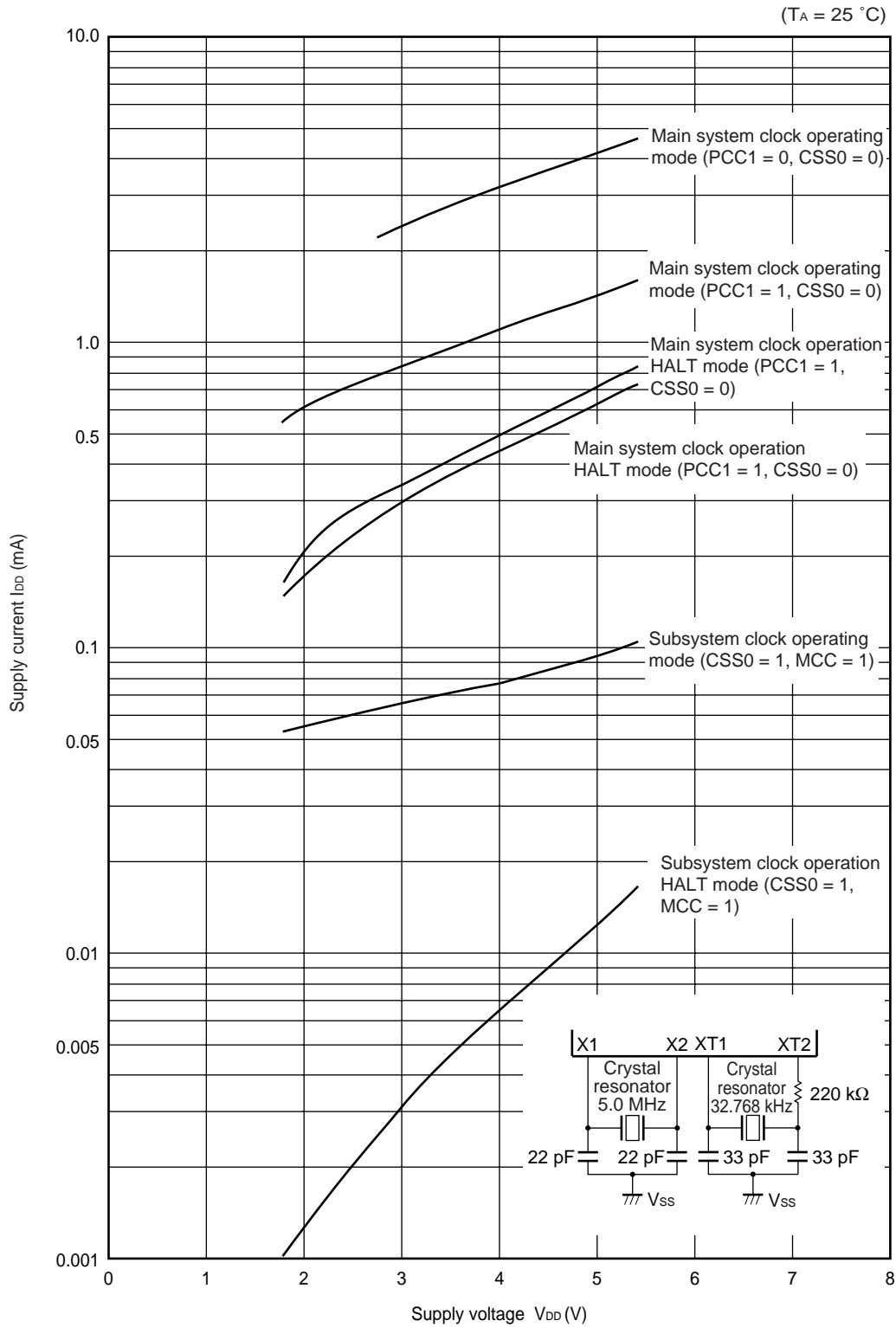
Data Retention Timing (STOP Mode Release by RESET)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



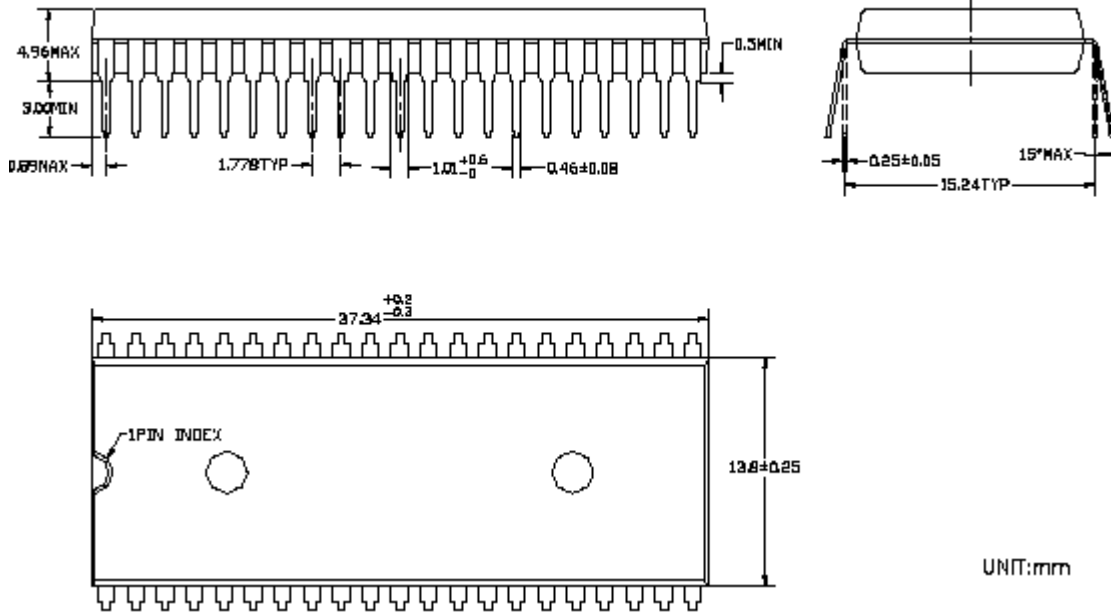
8. CHARACTERISTICS CURVES



9. PACKAGE DRAWING

42 pin Shrink DIP(600mil)

SDIP42PIN Package



10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9177 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F9177CU: 42-pin plastic shrink DIP (600mil)

Soldering Method	Soldering Conditions
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per each pin)

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DIFFERENCES BETWEEN μPD78F9177 AND MASK ROM VERSIONS

The μPD78F9177 is flash memory version of the Mask ROM version. The differences between the μPD78F9177 and the Mask ROM versions are shown in Table A-1.

Table A-1. Differences between μPD78F9177, 78F9177Y and Mask ROM Versions

Product Name		Flash Memory Version	Mask ROM Version
		μPD78F9177	μPD789166
Internal memory	ROM	24 KB	16 KB
	High-speed RAM	512 bytes	
V _{PP} pin		Provided	Not provided
Pull-up resistor		17 (Software control)	21 (Software control: 17, mask option specification: 4)
A/D resolution		10 bits	8 bits
Electrical specifications		See the relevant data sheet	

- Cautions**
1. There are differences in the amount of noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM versions, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering sample, ES) of the mask ROM version.
 2. When the μPD78F9177, a flash memory counterpart of the μPD789166 or μPD789167, is used, however, ADCR0 can be manipulated with an 8-bit memory manipulation instruction. In this case, use an object file assembled with the μPD789166 or μPD789167. The same is also true for the μPD78F9177Y, a flash memory counterpart of the μPD789166Y or μPD789167Y. When the μPD78F9177Y is used, ADCR0 can be manipulated with an 8-bit memory manipulation instruction. In this case, use an object file assembled with the μPD789166Y or μPD789167Y.

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78F9177 and μPD78F9177Y.

Language Processing Software

RA78K0S Notes 1, 2, 3	Assembler package common to 78K/0S Series
CC78K0S Notes 1, 2, 3	C compiler package common to 78K/0S Series
DF789177 Notes 1, 2, 3	Device file for μPD789167, 789177, 789167Y, and 789177Y Subseries
CC78K0S-L Notes 1, 2, 3	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3 Note 4 , PG-FP3)	Flash programmer dedicated for on-chip flash memory microcontrollers
★ FA-42CU/MI-FA-42CU	Flash memory programming adapter for 42-pin plastic shrink DIP

Debugging Tools(1/2)

IE-78K0S-NS In-circuit emulator	In-circuit emulator used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter	Adapter used to supply power from a 100- to 240-V AC outlet
IE-70000-98-IF-C Interface adapter	Adapter required when using the PC-9800 series (excluding notebook PCs) as the host machine for the IE-78K0S-NS (C bus supported)
IE-70000-CD-IF-A PC card/interface	PC card and interface cable required when using a notebook PC as the host machine for the IE-78K0S-NS (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter	Adapter required when using an IBM PC/AT™ or compatible as the host machine for the IE-78K0S-NS (ISA bus supported)
IE-70000-PCI-IF Interface adapter	Adapter required when using a PC equipped with a PCI bus as the host machine for the IE-78K0S-NS
IE-789177-NS-EM1 Emulation board	Emulation board used to emulate the peripheral hardware specific to the device. This is used in combination with the in-circuit emulator.
MI-PR9166CU Emulation probe	Board to connect an in-circuit emulator to the target system.

Debugging Tools(2/2)

MI-PR9166CU Emulation probe	Board to connect an in-circuit emulator to the target system.
SM78K0S Notes 1, 2	System simulator common to 78K/0S Series
ID78K0S-NS Notes 1, 2	Integrated debugger common to 78K/0S Series
DF789177 Notes 1, 2	Device file for μPD789167, 789177, 789167, and 789177Y Subseries

Real-Time OS

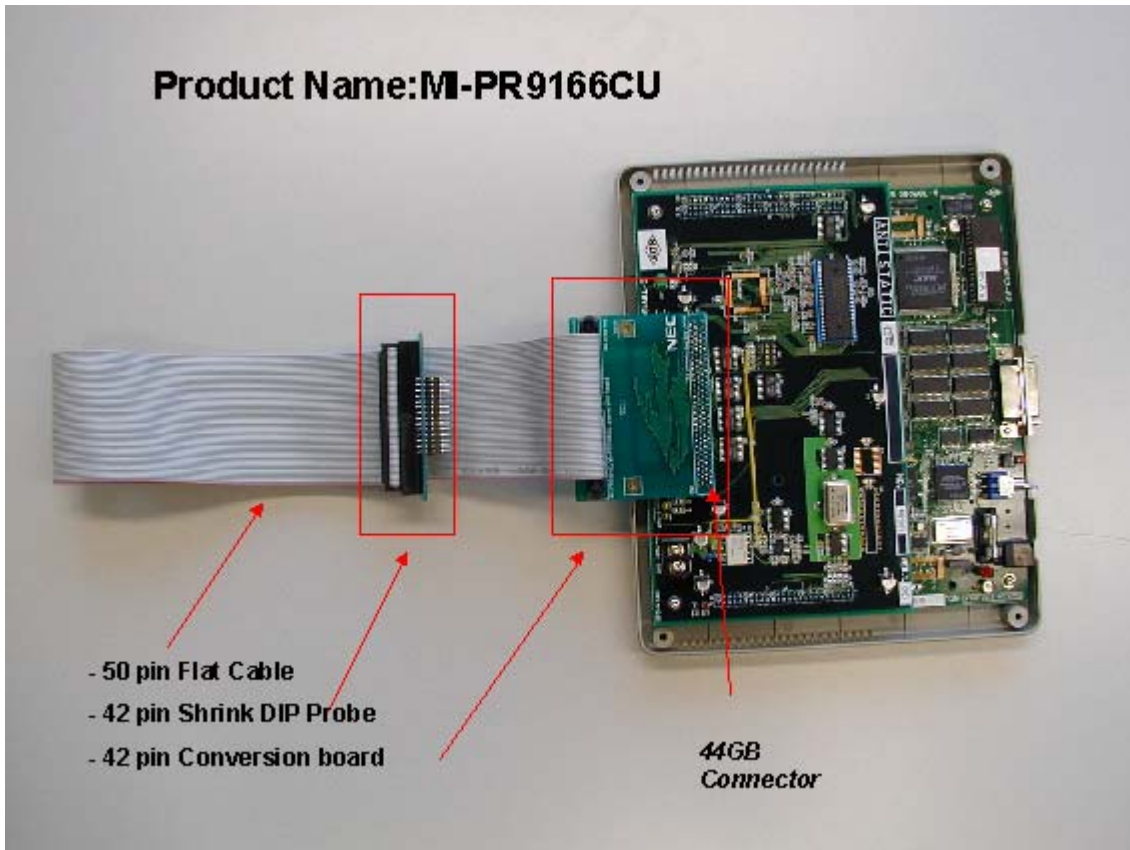
MX78K0S ^{Notes 1, 2}	OS for 78K/0S Series
-------------------------------	----------------------

- Notes**
1. Based on the PC-9800 series (Japanese Windows™)
 2. Based on IBM PC/AT and compatibles (Japanese Windows/English Windows)
 3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Soraris™), and NEWS™ (NEWS-OS™)
 4. Product made by and available from Naito Densai Machida Mfg. Co., Ltd. (+81-44-822-3813).
 5. Product made by TOKYO ELETECH CORPORATION.
 Refer to: Daimaru Kogyo, Ltd.
 Tokyo Electronic Division (+81-3-3820-7112)
 Osaka Electronic Division (+81-6-6244-6672)

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789177.

The MI-PR9116CU is as below.

The 120 pin connector on 42 pin conversion board should be connected to one for 44GB on EM board.



APPENDIX C. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD789166, 167, 176, 177, 166Y, 167Y, 176Y, 177Y, 166(A), 167(A), 176(A), 177(A), 166Y(A), 167Y(A), 176Y(A), 177Y(A) Data Sheet	U14017J	U14017E
μPD78F9177, 78F9177Y Data Sheet	U14022J	This manual
μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual	U14186J	U14186E
78K/0S Series Instruction User's Manual	U11047J	U11047E

Document Related to Development Tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows based	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Windows based	Reference	U12901J	U12901E
IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789177-NS-EM1 Emulation Board		U14621J	U14621E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
OS for 78K/0S Series MX78K0S	Fundamental	U12938J	U12938E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

The related document indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Differences between μPD789166CU, 78F9177CU, 789166GB, and 78F9177GB Subseries

The μPD789166CU, 78F9177CU, 789166GB, and 78F9177GB Subseries differ in their package type, A/D converter resolution etc.

Item		Subseries	μPD789166CU	μPD78F9177CU	μPD789166GB	μPD78F9177GB
Package			• 42-pin plastic shrink DIP		• 44-pin plastic LQFP	
A/D converter	Resolution		8 bits	10 bits	8 bits	10 bits
	Channel		6 ch		8 ch	
Port 6			Not provided		8 ch	
Operating Voltage Range			4.5-5.5V		1.8-5.5V	

Series Pin	μPD789166CU	μPD789166GB		μPD789166CU	μPD789166GB
	μPD78F9177CU	μPD78F9177GB		μPD78F9177CU	μPD78F9177GB
1	Vss0	P60/ANI0	23	ANI5	XT2
2	Vdd0	P61/ANI1	24	Avss	XT1
3	TI80/SS20/P25	P62/ANI2	25	P10	RESET
4	TO80/P26	P63/ANI3	26	P11	X2
5	P00	P64/ANI4	27	P30	X1
6	P01	P65/ANI5	28	P31/CPT90/INTP0/TI81	Vss0
7	P02	P66/ANI6	29	P32	Vdd0
8	P03	P67/ANI7	30	P33/TO82/INTP3/BZO90	P25/TI80/SS20
9	P04	Avss	31	P20/SCK20/ASCK20	P26/TO80
10	Vss1	P10	32	Vdd1	P00
11	P05	P11	33	P21/SO20/TxD20	P01
12	P50	P30/INTP0/TI80/CPT90	34	P22/SI20/RxD20	P02
13	P51	P31/INTP1/TO81	35	P23	P03
14	P52	P32/INTP2/TO90	36	P24	P04
15	P53	P33/INTP3/TO82/BZO90	37	IC/Vpp	Vss1
16	Avvd	P20/SCK20/ASCK20	38	XT2	P05
17	Avref	Vdd1	39	XT1	P50
18	ANI0	P21/SI20/TxD20	40	RESET	P51
19	ANI1	P22/SI20/RxD20	41	X2	P52
20	ANI2	P23	42	X1	P53
21	ANI3	P24	43		Avdd
22	ANI4	IC0/Vpp	44		Avref

Please refer to the related DS/UM

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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 - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
 - NEC semiconductor products are classified into the following three quality grades:
"Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
 - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
- (Note)
- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
 - (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).