HN705/HN706
Low-cost, µP Supervisory Circuits

DESCRIPTION

The HN705/706 microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The HN705/706 provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual-reset input.

Two supply-voltage monitor levels are available: The HN705 generate a reset pulse when the supply voltage drops below 4.65V, while the HN706 generate a reset pulse below 4.40V.

Devices are available in 8-pin DIP, SO and compact 8-pin MicroSO packages.

FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Precision power supply monitor
  --4.65V threshold (HN705)
  --4.40V threshold (HN706)
- Debounced manual reset input
- Voltage monitor
  --1.25V threshold
  --Battery monitor / Auxiliary supply monitor
- Watchdog timer
- 200ms reset pulse width
- Eliminates the need for discrete components
- Industrial temperature range -40 °C to +85 °C
- The HN705/706 is a plug-in replacement of the MAX705/706, DS1705/1706, IMP705/706, ADM705/706, MIC705/706 and SP705/706

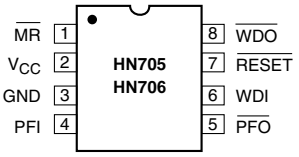
APPLICATIONS

- Microprocessor Systems
- PDA and portable Equipment
- Computers
- Controllers
- Wireless communication systems
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

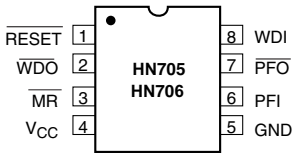
ORDERING INFORMATION

PART NO.	TEMP. RANGE (°C)	PACKAGE
HN705EN	-40 – 85 °C	8-Pin DIP
HN705EM	-40 – 85 °C	8-Pin SO
HN705EU	-40 – 85 °C	8-Pin MicroSO
HN705EX	-40 – 85 °C	Dice
HN706EN	-40 – 85 °C	8-Pin DIP
HN706EM	-40 – 85 °C	8-Pin SO
HN706EU	-40 – 85 °C	8-Pin MicroSO
HN706EX	-40 – 85 °C	Dice

PIN CONFIGURATION



DIP / SO

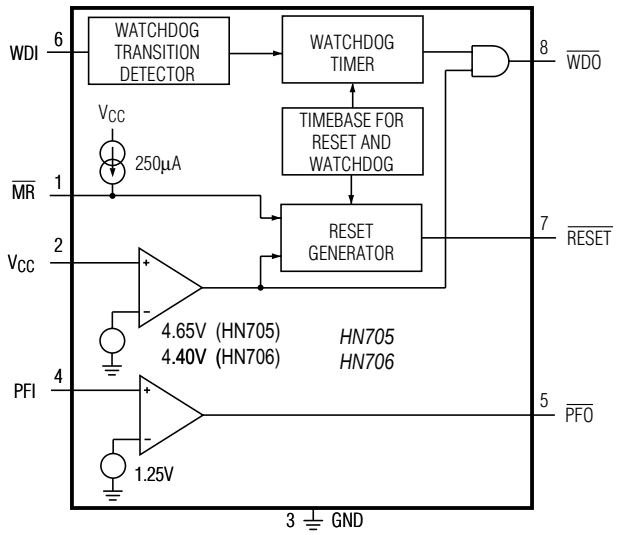


MicroSO

PIN CONFIGURATION

DIP/SO	MicroSO	Name	Function
1	3	$\overline{MR}$	Manual RESET input. The active LOW input triggers a reset pulse. A 250µA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch.
2	4	Vcc	+5V power supply input.
3	5	GND	Ground reference for all signals.
4	6	PFI	Power-fail voltage monitor input. With PFI less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to ground or V_{CC} when not used.
5	7	$\overline{PFO}$	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6sec at WDI allows the internal timer to run-out, setting WDO LOW. The internal watchdog timer clears when: RESET is asserted; or WDI sees a rising or falling edge.
7	1	$\overline{RESET}$	Active-LOW reset output. Pulses LOW for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (HN705: 4.65V, HN706: 4.40V). RESET remains LOW for 200ms after V_{CC} rises above the RESET threshold or MR goes from LOW to HIGH. A watchdog timeout will not trigger RESET unless WDO is connected to MR.
8	2	$\overline{WDO}$	Watchdog output. WDO pulls LOW when the 1.6 sec internal watchdog timer times-out, remains active (low) for a minimum of 130 ms, and does not go HIGH until the watchdog is cleared.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–60°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, Vcc=4.75 to 5.5V for the HN705, Vcc=4.5 to 5.5V for the HN706 and over -40°C to +85°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		1.2		5.5	V
Supply Current	I_{SUPPLY}			350		µA
Reset Threshold	V_{RT}	HN705	4.50	4.65	4.75	V
		HN706	4.25	4.40	4.50	
Reset Threshold Hysteresis				40		mV
RESET Pulse Width	t_{RS}		130	205	285	ms
RESET Output Voltage		I_{SOUCEL} =500µA	V_{CC}–0.3V	V_{CC}–0.1V		V
Watchdog Timeout Period	t_{WD}		1.0	1.6	2.2	s
WDI Pulse Width	t_{WP}	V_{IL} =0.4V, V_{IH} =0.8V	10			ns
WDI Input Threshold	V_{IL}	V_{CC} =5V	–0.03		+0.5	V
	V_{IH}		2.0		V_{CC}+0.3	
WDI Input Current		V_{CC} =5V	10		100	µA
$\overline{WDO}$ Output Voltage	V_{OH}	I_{SOUCEL} =500µA	V_{CC}–0.3V	V_{CC}–0.1V		V
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ =0V	50	250	450	µA
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ Input Threshold	V_{IL}		–0.03		+0.5	V
	V_{IH}		2.0		V_{CC}+0.3	
$\overline{MR}$ to Reset Out Delay	T_{MD}				250	ns
PFI Input Threshold		V_{CC} =5V	1.20	1.25	1.30	V
PFI Input Current			–1.0		+1.0	µA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOUCEL} =500µA	V_{CC}–0.3V	V_{CC}–0.1V		V

DETAILED DESCRIPTON

RESET Operation

The RESET signals are designed to start a µP / µC in a known state or return the system to a known state.

RESET is guaranteed to be LOW with V_{CC} above 1.2V. During a power-up sequence, RESET remains low until the supply rises above the threshold level, either 4.65V or 4.40V. RESET goes high approximately 200ms after crossing the threshold.

During power-down, RESET goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.5V with V_{CC} above 1.2V.

In a brownout situation where V_{CC} falls below the threshold level, RESET pulses low. If a brownout occurs during an already-initiated reset, the pulse will continue for a minimum of 130ms.

Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output (PFO) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the PFO output to transit LOW. Normally PFO interrupts the processor so the system can be shut down in a controlled manner.

Manual Reset (MR)

The active-LOW manual reset input is internally pulled up to V_{CC} with an internal impedance of 40KΩ typical and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 130ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output (WDO) and MR, a watchdog timeout forces RESET to be generated.

Watchdog Timer

The watchdog timer function forces WDO signals active when the WDI input is not clocked within the 1.6 second time-out period. Time-out of the watchdog starts when RST (or RST) becomes inactive. If a high-to-low transition occurs on the WDI input pin prior to time-out, the watchdog timer is reset and begins to time out again. If the watchdog timer is allowed to time out, the WDO signal is driven active (low) for a minimum of 130 ms. The WDI input can be derived from many microprocessor outputs. The typical signals used are the microprocessors address signals, data signals, or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time out, a high-to-low transition must occur at or less than the minimum watchdog time-out of 1 second.

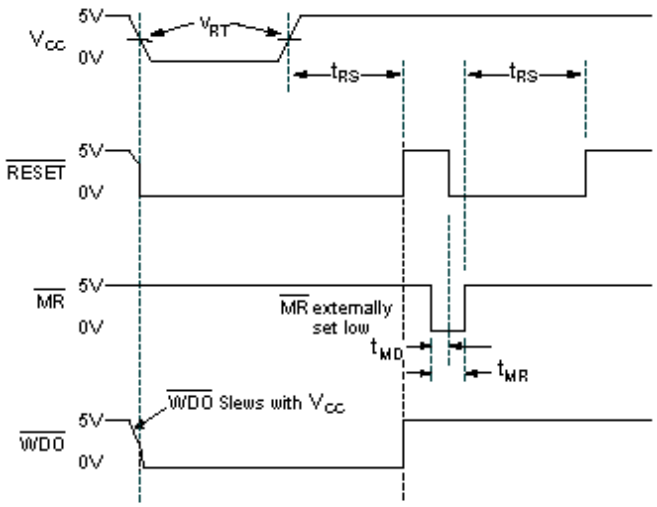


Figure 1. Power-down and Manual Reset

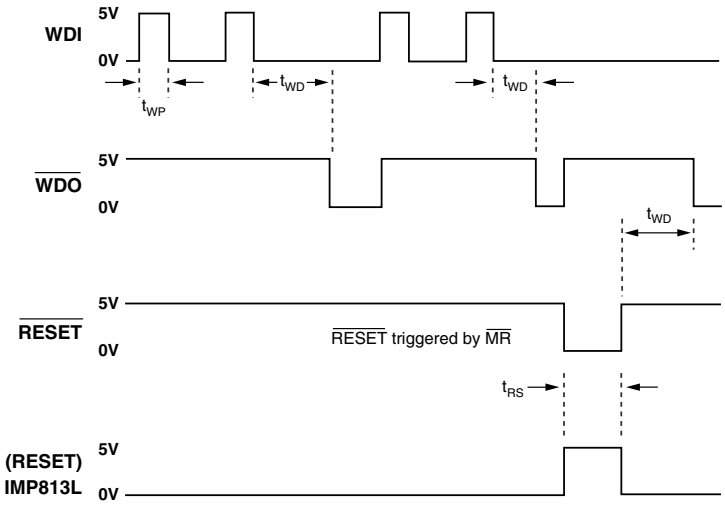


Figure 2. Watchdog Timing

APPLICATION INFORMATION

Ensuring That $\overline{\text{RESET}}$ is Valid Down to V_{CC} = 0V

When V_{CC} falls below 1.1V, the HN705/706 $\overline{\text{RESET}}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{\text{RESET}}$ to the wrong state, a pull-down resistor should be connected to the $\overline{\text{RESET}}$ pin, thus draining such charges to ground and holding $\overline{\text{RESET}}$ low. The resistor value is not critical. A 100kΩ resistor will pull $\overline{\text{RESET}}$ to ground without loading it.

Bi-directional Reset Pin Interfacing

The HN705/706 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the $\overline{\text{RESET}}$ output and the µP / µC bi-directional $\overline{\text{RESET}}$ pin.

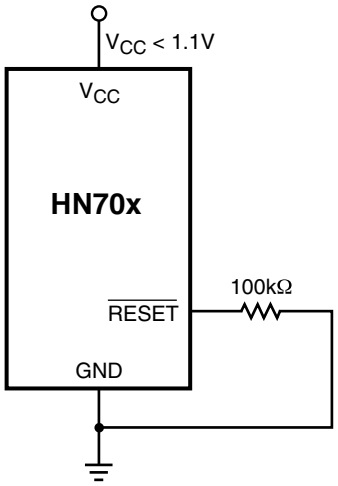


Figure 3. Ensuring That RESET is Valid Down to V_{CC} = 0V

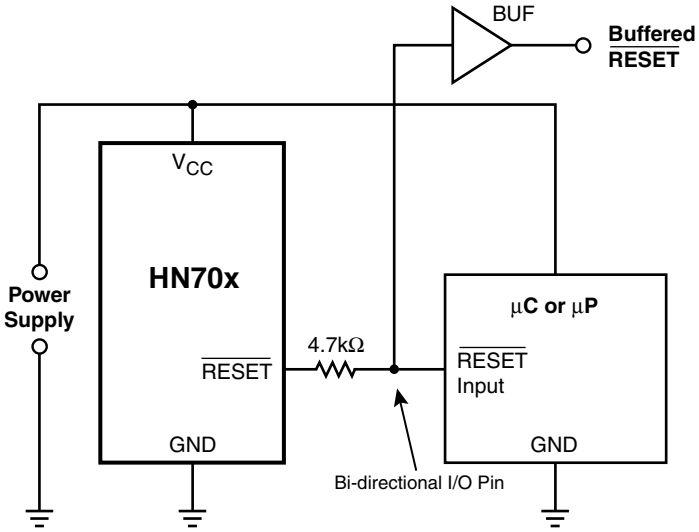


Figure 4. Bi-directional Reset Pin Interfacing

Monitoring Voltages Other Than V_{CC}

The HN705/706 can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the Power Fail input, PFI, the $\overline{PFO}$ (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and $\overline{PFO}$ pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a $\overline{RESET}$ in addition to the $\overline{PFO}$ flag, this may be achieved by connecting the $\overline{PFO}$ output to $\overline{MR}$.

Monitoring a Negative Voltage

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, $\overline{PFO}$ will be LOW, and when the negative rail is failing (not negative enough), $\overline{PFO}$ goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The $\overline{RESET}$ output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the V_{CC} line, the PFI threshold tolerance, and the resistors.

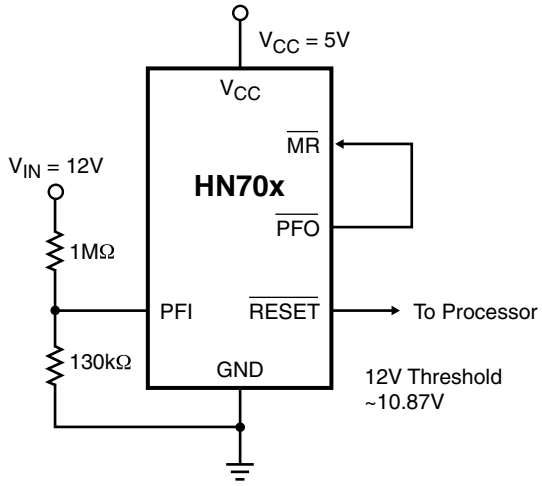


Figure 5. Monitoring Voltages Other Than V_{CC}

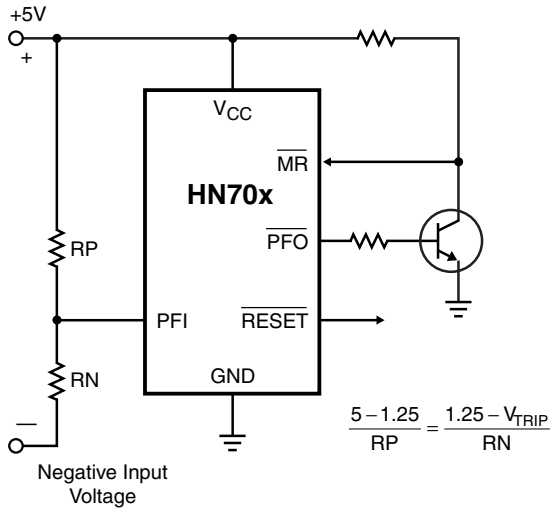
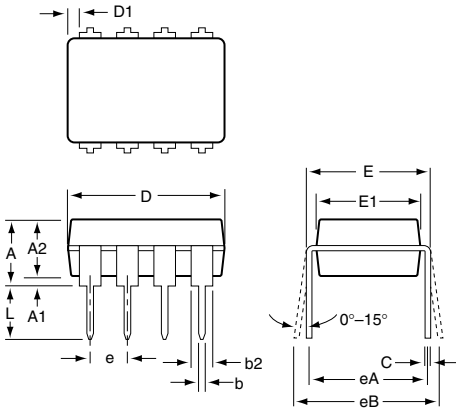


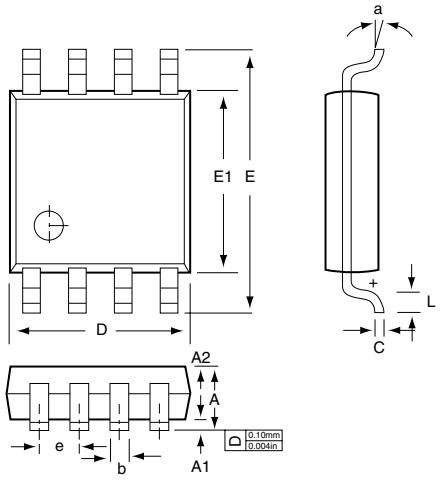
Figure 6. Monitoring a Negative Voltage

Package Dimensions

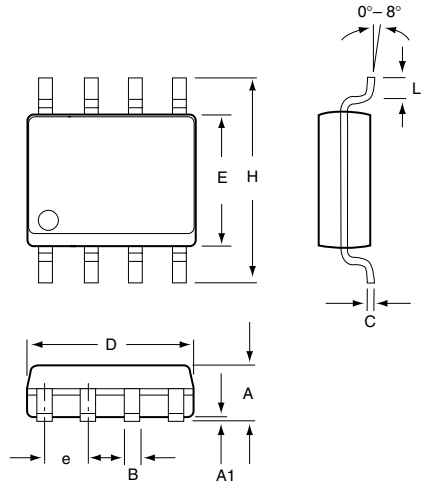
Plastic DIP (8-Pin)



MicroSO (8-Pin)



SO (8-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
Plastic DIP (8-Pin)				
A	———	0.210	——	5.33
A1	0.015	———	0.38	———
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	———	0.13	———
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	———	2.54	
eA	0.300	———	7.62	
eB	———	0.430	———	10.92
eC	———	0.060		
L	0.115	0.150	2.92	3.81
MicroSO (8-Pin)				
A	———	0.0433	——	1.10
A1	0.0020	0.0059	0.050	0.15
A2	0.0295	0.0374	0.75	0.95
b	0.0098	0.0157	0.25	0.40
C	0.0051	0.0091	0.13	0.23
D	0.1142	0.1220	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.193 BSC		4.90 BSC	
E1	0.1142	0.1220	2.90	3.10
L	0.0157	0.0276	0.40	0.70
a	0°	6°	0°	6°
SO (8-Pin)				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	5.00