ICL7135
4½ Digit Analog-To-Digital Converter

1. DESCRIPTION

The ICL7135 is 4 1/2-digit, dual-slope-integrating, analog-to-digital converter (ADC) designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs B1, B2, B4, and B8 provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135 offers 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10µV and zero drift is less than 0.5 µV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ±1 count.

The BUSY, STROBE, RUN/HOLD, OVER RANGE, and UNDER RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer through universal asynchronous receiver transmitters (UARTs).

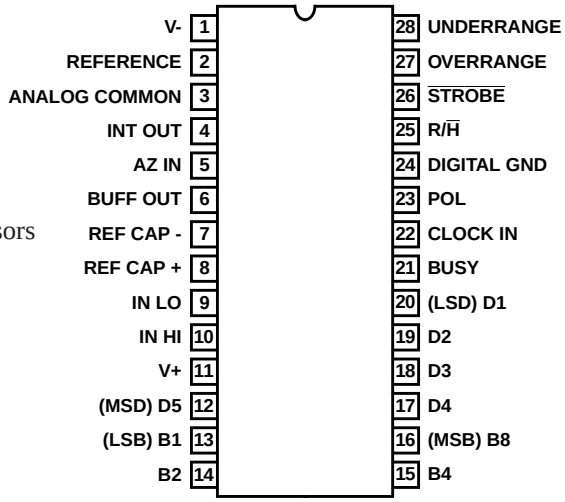
2. FEATURES

- Zero Reading for 0V Input
- Precision Null Detection With True Polarity at Zero
- 1pA Typical Input Leakage Current
- True Differential Input
- Multiplexed Binary-Coded-Decimal (BCD) Outputs
- Low Rollover Error: ±1 Count Max
- Control Signals Allow Interfacing With UARTs or Microprocessors
- Autoranging Capability With Over-and Under-Range Signals
- TTL-Compatible Outputs

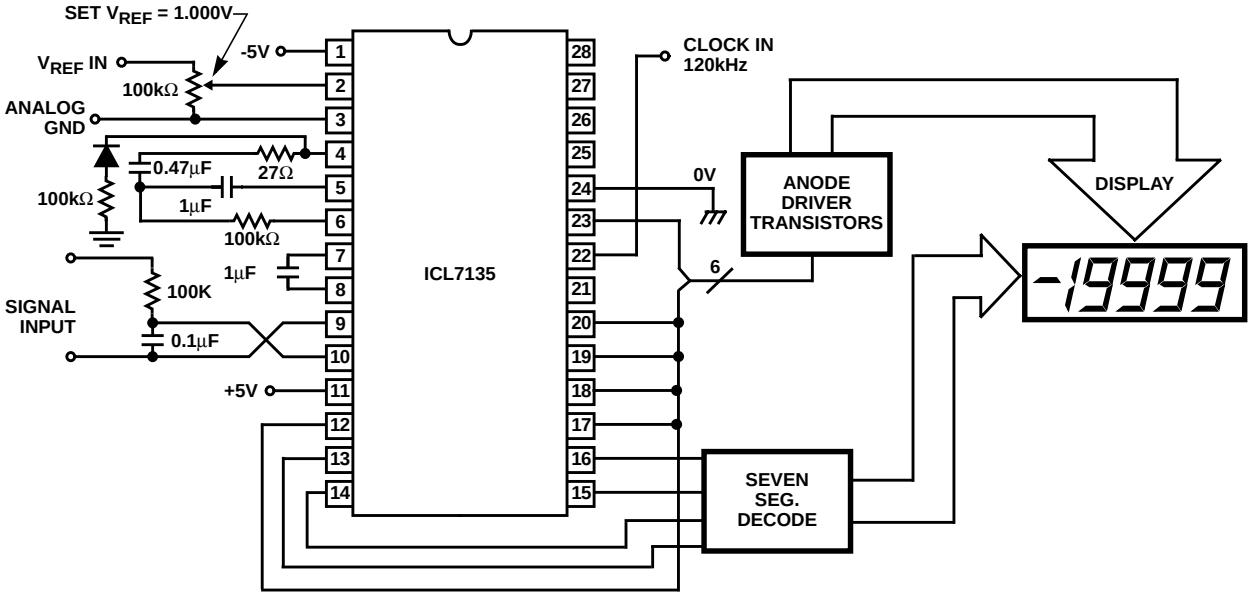
Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE
ICL7135CPI	0 – 70 °C	28 Ld. PDIP
ICL7135CM	0 – 70 °C	28 Ld. SOP28

DIP28 OR SOP28 PACKAGE
(TOP VIEW)



Typical Application Schematic



3. ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_+	+6	V
	V_-	-9	V
Analog Input Voltage (Either Input) (Note1)		V_+ to V_-	
Reference Input Voltage (Either Input)		V_+ to V_-	
Clock Input Voltage		GND to V_+	
Operating Free-Air Temperature Range	T_A	0 to 70	°C

4. ELECTRICAL CHARACTERISTICS

(V^+ = 5V; V^- = -5V; V_{REF} = 1.000V; f_{CLK} =120kHz, Ta = 25°C (unless otherwise specified)

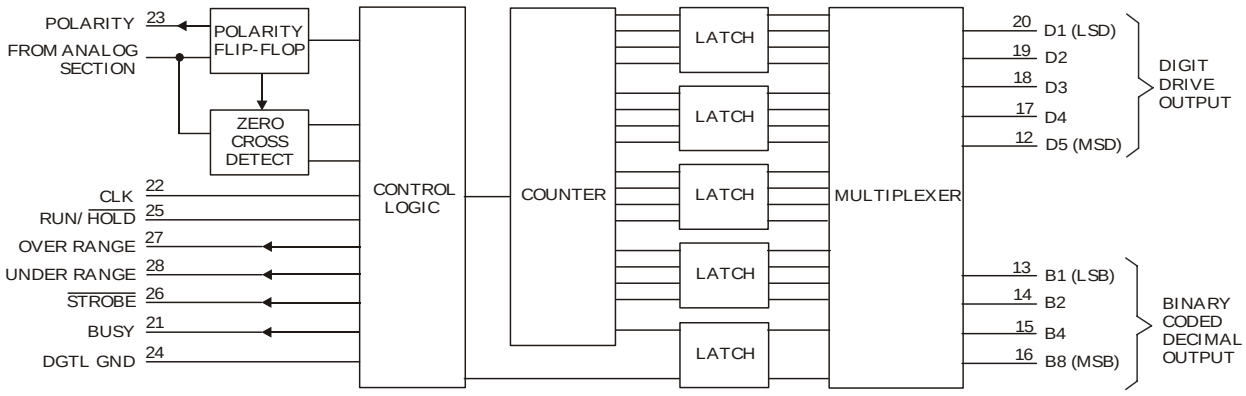
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V^+		4		6	V
	V^-		-3		-8	
High-Level Input Voltage, CLK, RUN/HOLD	V_{IH}		2.8			V
Low-Level Input Voltage, CLK, RUN/HOLD	V_{IL}				0.8	V
Clock Frequency	f_{CLK}			2000	1200	kHz
High-Level Output Voltage						
D1-D5, B1, B2, B4, B8	V_{OH}	I_O = -1mA	2.4		5	V
Other Outputs		I_O = -10μA	4,9		5	
Low-Level Output Voltage	V_{OL}	I_O = 1.6mA			0.4	V
Peak-to-peak Output Noise Voltage (Note1)	$V_{ON(PP)}$	V_{ID}=0, Full scale=2V		15		μV
Zero-reading Temperature Coefficient of Output Voltage	α_{VO}	V_{ID}=0		0.5	2	μV/°C
High-Level Input Current	I_{IH}	V_I=5V		0.1	10	μA
Low-Level Input Current	I_{IL}	V_I=0V		-0.02	-0.1	mA
Input Leakage Current, IN- and IN+	I_I	V_{ID}=0		1	10	pA
Positive Supply Current	I^+	f_{CLK}=0		1	2	mA
Negative Supply Current	I^-	f_{CLK}=0		-0.8	-2	mA
Full-scale Temperature Coefficient (Note 2)	αFS	VID=2V			5	ppm/ °C
Linearity Error	EL	-2V ≤ VID ≤ 2V		0.5		count
Differential Linearity Error (Note 3)	ED	-2V ≤ VID ≤ 2V		0.01		LSB
Full-scale Symmetry Error (Rollover Error) (Note 4)	EFS	VID= ± 2V		0.5	1	count
Display Reading with 0V Input		VID=0	-0.0000	±0.0000	0.0000	Digital Reading
Display Reading in Ratiometric Operation		VID=VREF	0.9997	0.9999	1.0003	Digital Reading

NOTES:

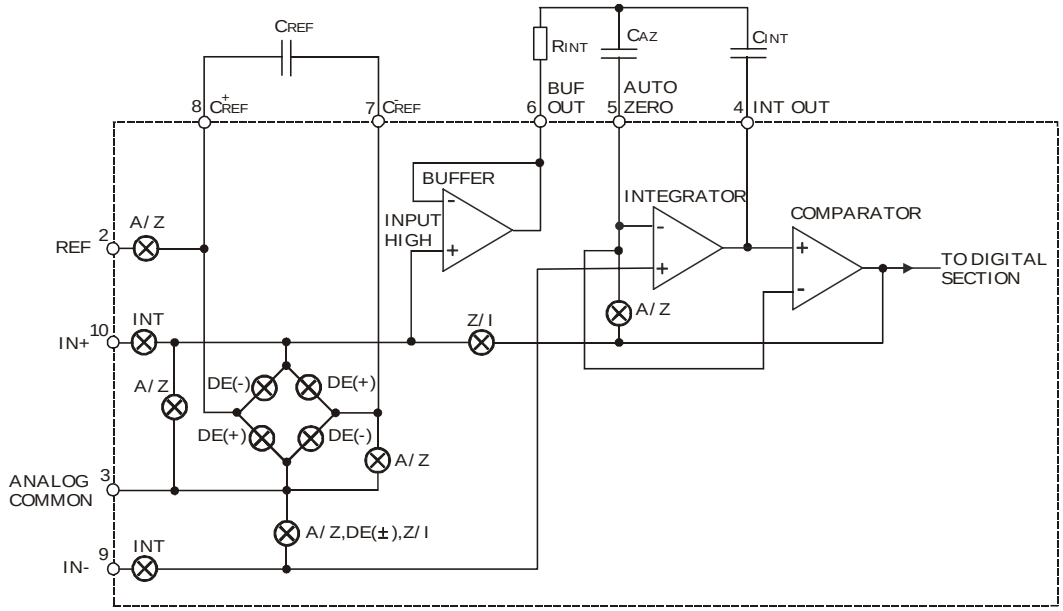
1. This is the peak-to-peak value that is not exceeded 95% of the time.
2. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
3. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
4. Rollover error is the difference between the absolute values of the conversion for 2V and -2V.

5. FUNCTIONAL BLOCK DIAGRAM

DIGITAL SECTION



ANALOG SECTION



6. TIMING DIAGRAMS

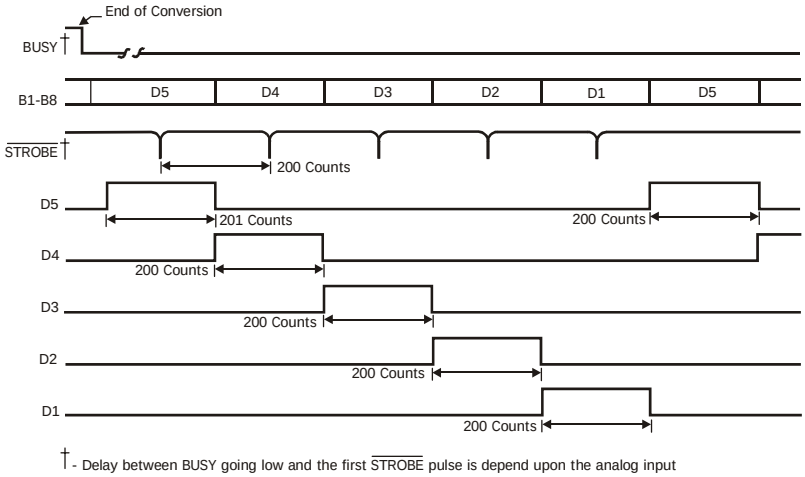


Fig.1.

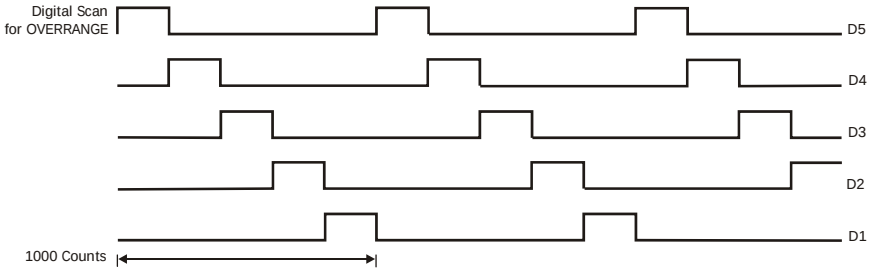


Fig.2.

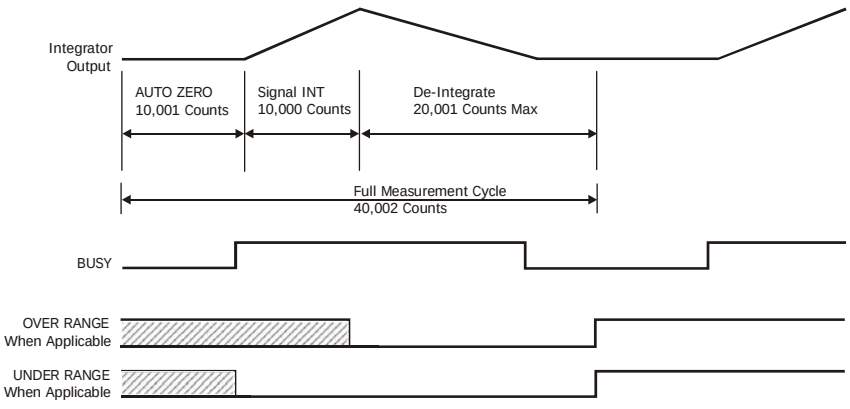


Fig.3.

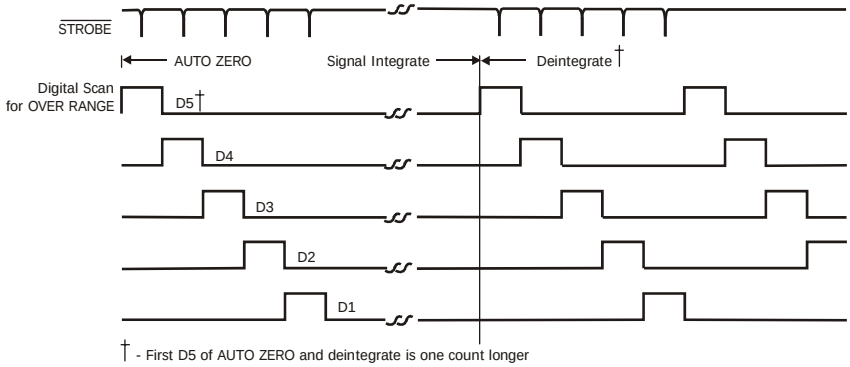


Fig.4.

7. PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135 consists of the following four phases.

1. Auto-Zero Phase.
The internal IN+ and IN- inputs are disconnected from the terminals and internally connected to ANALOG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 µV.

2. Signal Integrate Phase.
The auto-zero loop is opened and the internal IN+ and IN- inputs are connected to the external terminals.
The differential voltage between these inputs is integrated for a fixed period of time. When the input signal has no return with respect to the converter power supply, IN- can be tied to ANALOG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.

3. Deintegrate Phase.
The reference is used to perform the deintegrate task. The internal IN- is internally connected to ANALOG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal ensures that the capacitor is connected with the correct polarity so that the integrator output polarity returns to zero. The time required for the output to return to zero is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation 10000 x (V_{ID}/V_{REF}). The maximum or full-scale conversion occurs when V_{ID} is two times V_{REF}.

4. Zero Integrator Phase.
The internal IN- is connected to ANALOG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically, this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

8. DESCRIPTION OF ANALOG CIRCUITS

• Input Signal Range

The common mode range of the input amplifier extends from 1V above the negative supply to 1V below the positive supply. Within this range, the common-mode rejection ratio (CMRR) is typically 86 dB. Both differential and common-mode voltages cause the integrator output to swing. Therefore, care must be exercised to ensure that the integrator output does not become saturated.

• Analog Common

Analog common (ANALOG COMMON) is connected to the internal IN- during the auto-zero, deintegrate, and zero integrator phases. When IN- is connected to a voltage that is different from analog common during the signal integrate phase, the resulting common-mode voltage is rejected by the amplifier. However, in most applications, IN- is set at a known fixed voltage (i.e., power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. Removing the common-mode voltage in this manner slightly increases conversion accuracy.

• Reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference.

9. DESCRIPTION OF DIGITAL CIRCUITS

• RUN/HOLD Input

When RUN/HOLD is high or open, the device continuously performs measurement cycles every 40002 clock pulses. When this input is taken low, the integrated circuit continues to perform the ongoing measurement cycle and then hold the conversion reading for as long as the terminal is held low. When the terminal is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) initiates a new measurement cycle. When this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first STROBE pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurement after the first STROBE pulse.

• STROBE Output

Negative going pulses from this output transfer the BCD conversion data to external latches, UARTs, or microprocessors. At the end of the measurement cycle, STROBE goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD terminals. After the first 101 counts, halfway through the duration of output D1-D5 going high, the STROBE terminal goes low for 1/2 clock pulse width. The placement of the STROBE pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the STROBE pulse also ensures that the BCD bits for the second MSD are not yet competing for the BCD lines and latching of the correct bits is ensured.

The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines continue scanning without the inclusion of STROBE pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

• BUSY Output

The BUSY output goes high at the beginning of the signal integrate phase. BUSY remains high until the first clock pulse after zero crossing or at the end of the measurement cycle when an over-range condition occurs. It is possible to use the BUSY terminal to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses that occur during the deintegrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

• OVER-RANGE Output

When an over-range condition occurs, this terminal goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER RANGE output goes high at the end of BUSY and goes low at the beginning of the deintegrate phase in the next measurement cycle.

• UNDER-RANGE Output

At the end of the BUSY signal, this terminal goes high when the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

• POLARITY Output

The POLARITY output is high for a positive input signal and updates at the beginning of each deintegrate phase. The polarity output is valid for all inputs including ±0 and OVER RANGE signals.

• Digit-Drive (D1, D2, D4 and D5) Outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit-drive outputs are blanked from the end of the strobe sequence until the beginning of the deintegrate phase (when the sequential digit-drive activation begins again). The blanking activity during an over-range condition can cause the display to flash and indicate the over-range condition.

• BCD Outputs

The BCD bits (B1, B2, B4 and B8) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate digit-drive line for the given digit is activated.

10. SYSTEM ASPECTS

• Integrating Resistor

The value of the integrating resistor (RINT) is determined by the full-scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 µA of current with negligible nonlinearity. The equation for determining the value of this resistor is:

$$R_{INT} = \frac{\text{FullScaleVoltage}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40µA yields good results. However, the nominal and recommended current is 20µA.

• Integrating Capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. When the amplifier output is within 0.3V of either supply, saturation occurs. With ±5V supplies and ANALOG COMMON connected to ground, the designer should design for a ±3.5V to ±4V integrating amplifier swing. A nominal capacitor value is 0.47 µF. The equation for determining the value of the integrating capacitor (C_{INT}) is:

$$C_{INT} = \frac{10000 \times \text{Clock Peruiod} \times I_{INT}}{\text{Integrator Output Voltage Swing}}$$

where I_{INT} is nominally 20µA.
Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor that is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and deintegrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and polycarbonate capacitors have higher dielectric absorption, but also work well.

• Auto-Zero and Reference Capacitor

Large capacitors tend to reduce noise in the system. Dielectric absorption is unimportant except during power up or overload recovery. Typical values are 1µF.

• Reference Voltage

For high-accuracy absolute measurements, a high quality reference should be used.

• Rollover Resistor and Diode

The ICL7135 has a small rollover error; however, it can be corrected. The correction is to connect the cathode of any silicon diode to INT OUT and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions, the resistor value is 100kΩ. This value may be changed to correct any rollover error that has not been corrected. In many non-critical applications the resistor and diode are not needed.

• Maximum Clock Frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3-µs delay. Therefore, with a 160kHz clock frequency (6-µs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading changes from 0 to 1 with a 50µV input, 1 to 2 with a 150µV input, 2 to 3 with a 250µV input, etc. This transition at midpoint is desirable; however, when the clock frequency is increased appreciably above 160kHz, the instrument flashes 1 on noise peaks even when the input is shorted. The above transition points assume a 2V input range is equivalent to 20000 clock cycles.

When the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1MHz are possible since nonlinearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay are a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the deintegrate phase, and thus compensates for the comparator delay. This series resistor should be 10Ω to 50Ω . This approach allows clock frequencies up to 480kHz.

• Minimum Clock Frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 µs are not influenced by leakage error.

• Rejection of 50-Hz or 60-Hz Pickup

To maximize the rejection of 50Hz or 60Hz pickup, the clock frequency should be chosen so that an integral multiple of 50Hz or 60-Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies that can be used are:
50Hz: 250, 166.66, 125, 100kHz, etc.
60Hz: 300, 200, 150, 120, 100, 40, 33.33kHz, etc.

• Zero-Crossing Flip-Flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle has occurred, so any comparator transients that result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the deintegrate phase.
Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

• Noise

The peak-to-peak noise around zero is approximately 15µV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30µV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

• Analog and Digital Grounds

For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

• Power Supplies

The ICL7135 is designed to work with ±5V power supplies. However, 5V operation is possible when the input signal does not vary more than ±1.5V from midsupply.